Still being revised !!!!!!!!!!!!!!!!

SVX4 User's Manual

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Abstract: We present and describe the operation of the SVX4 chip.

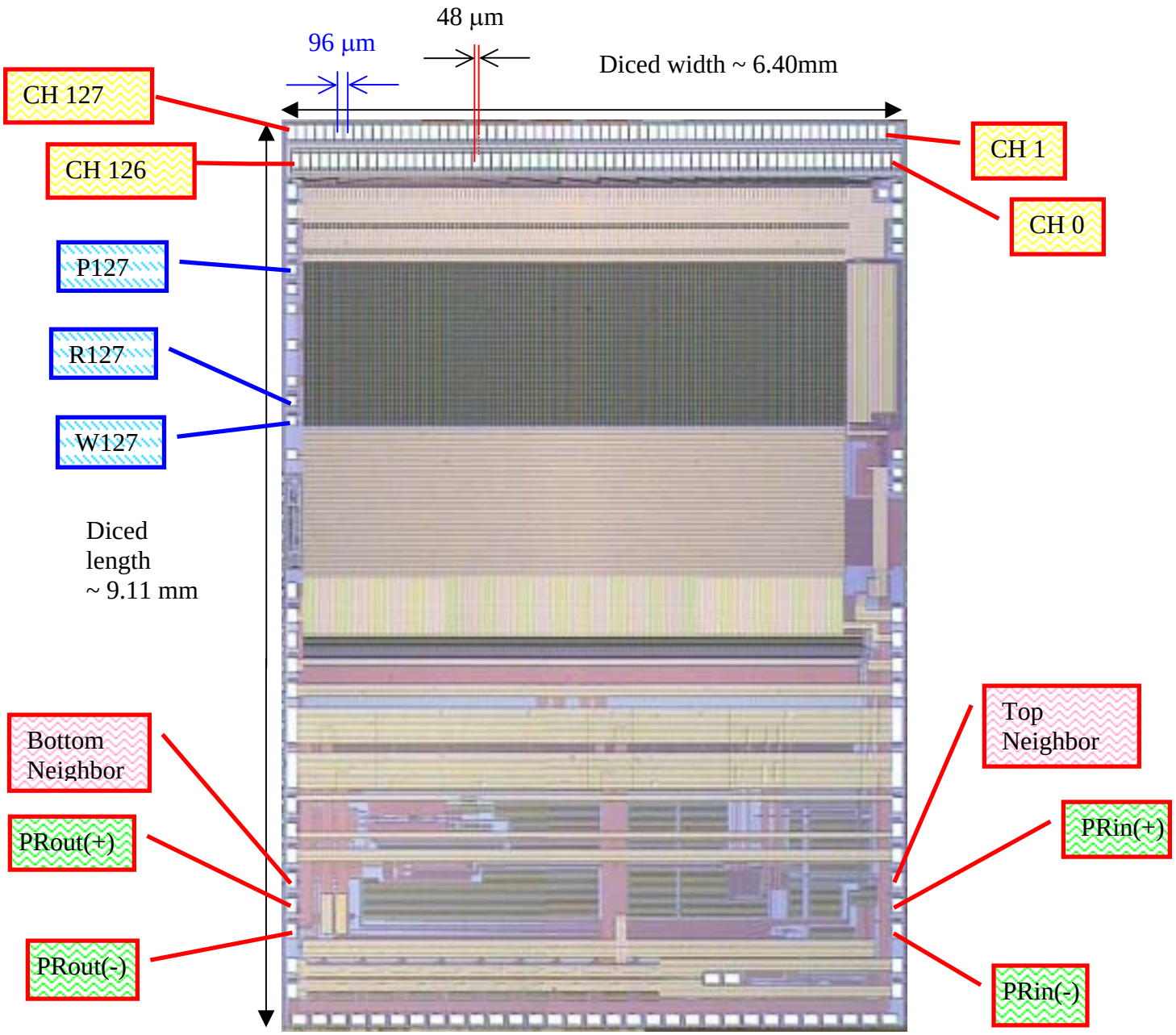

Figure 1 An actual picture of the SVX4 chip. The bottom of the picture is the back-end of the chip and the upper half is the front-end. The 128 input pads can be seen at the top of the picture. The Priority in/out, and Top/Bottom Neighbor are indicated at the bottom of the picture. The three buffered diagnostic analog probe points of the last channel (127) are also shown on the left. This chip is fabricated with the 0.25 micron TSMC process on 300-micron thick silicon.

1. Introduction

The SVX4 is a custom 128-channel analog to digital converter chip used by D∅ and CDF in Run IIb to read out their respective silicon strip detectors. Each channel consists of an integrator (Front-End device, or FE) and a digitize/readout section (Back-End device, or BE). The input to each channel is sampled and temporarily stored in its own storage capacitor. Upon receiving a trigger signal, the relevant pipeline cell is reserved. Subsequent signals cause reserved cells to be digitized by a 128 parallel channel Wilkinson type 8-bit ADC, and then readout in byte-serial mode with optional zero suppression (sparsification). Salient features include (1) operation in either D∅ mode or CDF mode (CDF mode features "dead timeless operation" or continued acquisition during digitization and readout), (2) adjustable, loadable control parameters, including the integrator bandwidth and ADC polarity (only one input charge polarity will be used for Run IIb, but this feature remains for diagnostic purposes), (3) sparsified readout with nearest neighbor logic, (4) built-in charge injection with the ability for external voltage overriding for testing and calibration, and (5) a channel mask that is used for either charge injection or for masking of channels with excessive DC current input during chip operation. This document is meant to familiarize the user with the functionality of the SVX4 and goes on to include specifications, pin outs, timings and electrical information.

More information can be found under Marc Weber's page at LBL ; another repository of information is also in a folder in the FERMI Windows Domain. These links will be updated in the near future.

1.1 Silicon Strip Detectors for CDF and D0 for Run Iib

Both D0 and CDF for Run IIb have opted to use silicon strip detectors for their vertex detectors that are (1) single sided p-implant on n-type material, (2) 300 micrometers thick, (3) have typically a strip pitch of ~50 micrometers, (4) are resistively biased with bias resistors that are on the detector itself (R bias ~ 2 megohms), (5) are capacitively coupled to the readout chips with on board capacitors (that are formed by a dielectric/aluminum strip structure deposited on top of the p-implant strips, Ccoupling ~ 25 pF), and (6) are biased to full depletion by applying a positive potential to the n-side (ohmic, backplane) side of the detector and thus have the p-implant (junction) side at ground potential.

A simplified schematic is shown in Figure 2 . Ionizing particles traversing the depletion region of this backwards biased diode liberate electron-hole pairs and thus cause a short burst of charge to appear at the input capacitor. The first stage of the SVX4 chip is an integrating amplifier that collects the charge during a well defined period of time, which in the case of the two Tevatron experiments is roughly equal to the time between beam bunch crossings, and presents this integrated charge to a charge storing pipeline and ultimately to the digitizing circuit for digitization.

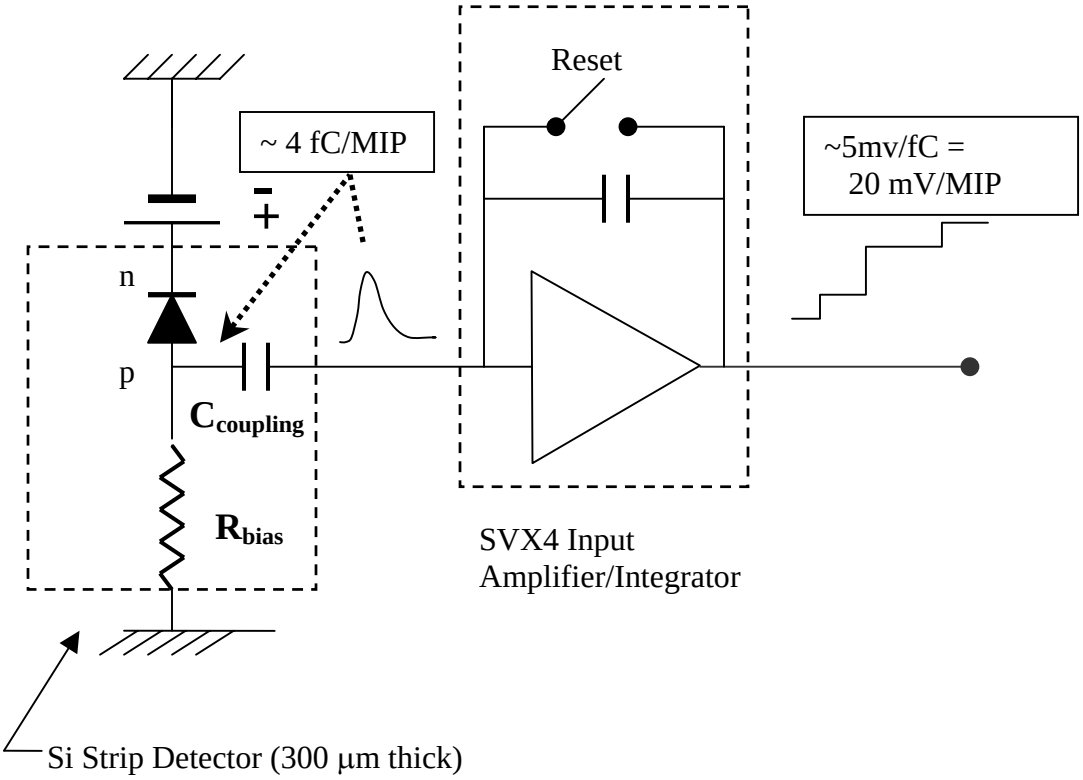

Figure 2- Block diagram of a Silicon Strip Detector and the front end of the SVX4 chip. The biasing scheme and polarities of the signals for the Run IIb vertex detectors of both CDF and D0 are indicated.

For completeness it should be noted that for normal incidence for a Minimum Ionizing Particle (MIP) and for a silicon detector thickness of 300 microns the expected signal is approximately 22000 electron-hole pairs, which corresponds to 3.5 fC . (Note that 1fC=6241e's, 1e=1.602x10^{-4} fC).

1.2 Historical Development

In the late 1980's, several versions of a fully custom chip called the SVX were built and tested (Refs. 1,2) As part of the Run IIa upgrade for D∅ the SVX2 and for CDF the SVX3 were designed to meet the needs of the experiments by a collaboration of engineers at Fermilab and Lawrence Berkeley Laboratory (Refs 1,2,3,4). Requirements dictated that the devices should be capable of operating at an interaction rate as fast as 132 nsec, that it have optimal performance for detector capacitances between 10 and 35 pF, and that it have an analog pipeline with a maximum delay of about 4 μsec to allow time to form a trigger signal.

For the SVX2 chip used by D0, when a trigger signal is received, data acquisition stops until the chip is completely read out. As plans for Run IIa evolved, dead time because an issue for CDF and the

development of the SVX3 with a dead timeless feature ensued. The SVX4, the successor design to the SVX3l, is a chip which can be used in either dead timeless mode (CDF) or in an arrested mode (D0) . A large effort and several iterations proved necessary to overcome digital-analog coupling issues seen in dead timeless operation.

The main features and specifications of the SVX4 are given below:

1. 128 channels per chip
2. Maximum interaction rate equal to 132 nsecs
3. Optimized for capacitive loads from 10-35 pF
4. Channel mask with dual functionality: used for either charge injection or masking channels with excessive DC current from the detector
5. Choice of operation in either D∅ or CDF mode using an external pad as selector
6. Selectable input bandwidth
7. Double correlated sampling (see section 2.2.1)
8. Large dynamic range on input integrator to minimize dead time due to pre-amplifier resets
9. Programmable analog pipeline (47 cells, 42 cells maximum depth for pipeline, 4 cells for trigger buffer, 1 cell for write amplifier pedestal)
10. Digitization of analog signals with up to 8 bits of resolution using a modified Wilkinson type ADC
11. Dynamic (real time) pedestal subtraction
12. Data sparsification (zero suppression)
13. Neighbor channel readout selection (cluster readout)
14. Low noise (S/N=10:1 to 20:1 for input capacitances from 35 pF to 10 pF for an input charge equivalent to 1 MIP = 4 fC)
15. Low power consumption (approximately 3 mW/channel) to minimize the cooling requirements
16. Operation with a single voltage source (even though two separate decoupled supplies for the analog and the digital portions of the chip may be required).
17. Operation compatible with single-sided AC coupled silicon strip detectors
18. Ability to inject charge for testing and calibration in each channel
19. Daisy chain operation capability
20. Parallel bus data readout
21. Integral Data Valid strobe signal in the data bus (OBDV)
22. Can be implemented in the TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 micron process which is inherently a radiation hard process

The document is arranged as follows: Section 2 gives a detailed description of the chip's operation, including timing diagrams, Section 3 defines the initialization bits in detail. Issues on measuring the performance of the chip in Section 4. The electrical specifications are given in Section 5 and Section 6 describes how to connect and mount chips. Section 7 lists a number of miscellaneous considerations. The appendices compare settings and measurements of the chip on several different test stands with those from the prototype DAQ system.

1.3 Simplified Operation

The SVX4 is comprised of 128 channels of identical electronics along with additional circuitry that is common to all channels. Figure 3 shows a simplified diagram of one of the identical channels of electronics and some of the common circuitry. Charge is received from the silicon strip detector via the input bond wire and integrated on a 220fF feedback capacitor, Cf, which sets the DC gain of the

input amplifier to be 5 mV/fC. In addition to the detector input, a separate 25fF test input capacitor, Ct, is connected to each integrator via a programmable switch. The capacitor allows each channel to be pulsed independently (synchronously with with a common control pulse) to study channel operation or provide simulated events to the SVX4 to the data acquisition system. The AC response of the front end electronics is determined primarily by the integrator response (there is no shaper). For different interaction times and input capacitances, the bandwidth of the preamplifier is adjusted by means of control registers to provide the optimal preamplifier output rise time and hence minimum noise.

The output of the preamplifier (integrator) feeds the analog pipeline which has a length of 46 cells, a number determined by the minimum interaction time and maximum required time delay. The pipeline has a fixed voltage gain of three determined by the ratio of the value of the input coupling capacitor, Cc, and the storage capacitors, Cn. The effective depth of the pipeline is the same for all channels and can be set via digital control to have any value from 1 to 42 samples. The pipeline operates by sequentially sampling the output of the preamplifier on one of 46 storage capacitors. After each interaction period, switch Sd in the pipeline resets the next sampling capacitor causing the output of the preamplifier to be stored on the coupling capacitor, Cc, and thus performing a double correlated sample on the preamplifier output (this way the integrator baseline does not matter, only the change in level during a given beam crossing is stored in the pipeline). The integrator output is allowed to build until it can be reset by switch Sa at a convenient time as shown in Figure 4.

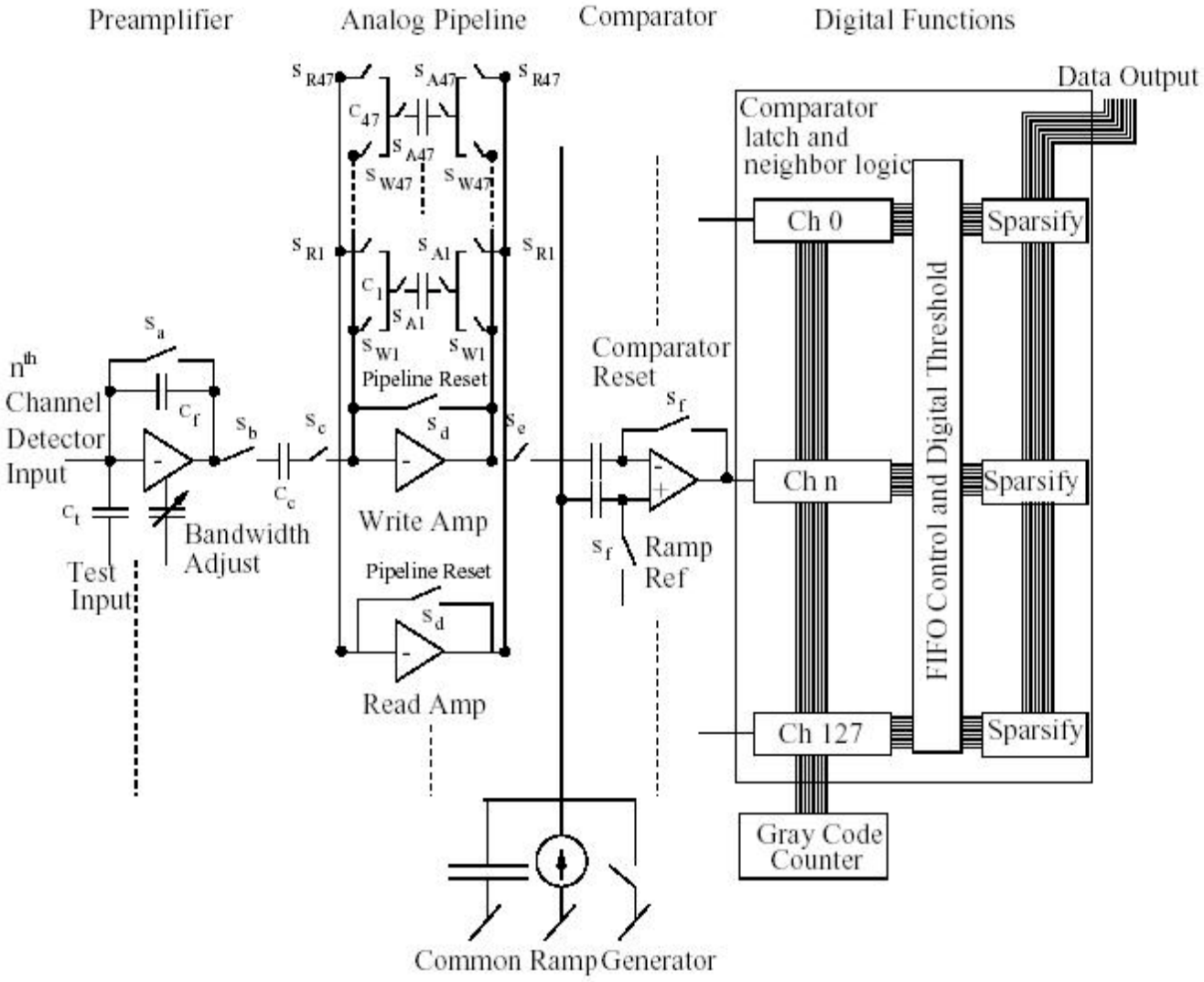

Figure 3 Simplified single channel block diagram.

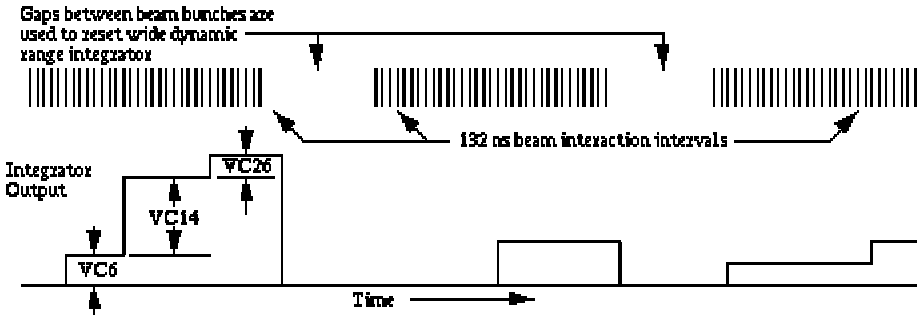

Figure 2 – Resetting Integrator Output During Large Beam Gap

Figure 4 Resetting integrator output during large beam gaps.

The voltage change indicated by VC6, VC14, and VC26 (which is indicative of charge injected at the input of the SVX at these three times) is stored on a sample capacitor for subsequent readout. Charge injection from opening Sd and the sample switches is stored on the sample capacitor along with the desired signal. These charge injection effects are compensated during the pipeline readout using a 47^{th} pipeline cell reserved exclusively for this purpose. Resetting a storage capacitor can be done in 20 ns. However, resetting the preamplifier requires a settling time of the order of 200 ns and is therefore reset during the major beam gaps in the main ring beam structure or at other times that do not interfere with normal data taking. The dynamic range of the preamplifier is 200 fC.

Readout of the SVX4 begins when a Level 1 Accept control signal (derived from the system trigger) is sent to the chip. Depending on which mode the chip is configured, two things can occur: 1) in D0mode, pipeline acquisition should stop and pipeline readout of the appropriate storage capacitor should begin and 2) in CDF mode, pipeline acquisition continues and the appropriate pipeline is stored in a secondary pipeline where it awaits the readout and digitization process.

When the proper control signals are sent to the chip for pipeline read out, a pedestal correction is performed on the stored signal in the pipeline to correct for variations in switch charge injection and other errors; this is accomplished by subtracting the value stored on the 47^{th} pipeline cell from the stored signal. The output of each pipeline feeds a Wilkinson type 8 bit ADC. The ADC is formed by a separate analog comparator, analog delay (which is used for dynamical pedestal subtraction), a counter latch for each channel and common ramp generator and Gray Code counter which is used for all of the channels. A digital conversion is initiated by activating the analog comparator for each channel and then starting the ramp generator and then the Gray Code counter. The ramp is applied to the analog comparator along with the input signal to be digitized. When the comparator output changes, the counter latch is set (after passing through the analog delay) which stores the output of the Gray Code counter for that channel. The number stored in the digital latch is a measure of the amount of charge that was integrated by the preamplifier from a given interaction. When the number in the Gray Code latch exceeds a programmed threshold setting, that channel is considered to have a hit and it is tagged for readout.

The SVX4 is designed to work with AC coupled single sided detectors, and is optimized for current pulses of the polarity shown in Figure 2, which we call positive polarity. It is able to accept negative polarity input signals but with a much more limited input range (see Ref xx). The functionality discussed below is only used for diagnostic purposes. Several signal inversions take place inside the SVX4 chip. The output of the preamplifier is inverted as shown in Figure 1 (e.g. the output signal level is negative going for positive input current and positive going for negative input current). The pipeline inverts the preamplifier signal. The technique used to read out the pipeline causes a third signal inversion to occur. Thus during pipeline readout which occurs prior to digitization, the signal level to the analog comparator is negative going for positive input current or positive going for negative input current.

For proper operation, externally programmed polarity signals are used to choose either positive or negative input operation for the chip. Three bits (Pipeline Readout Order, Ramp Polarity, Comparator Polarity) are provided for maximum flexibility to set levels inside the chip and establish the proper operation. The polarity signals perform three different functions inside the SVX4 chip. First Pipeline Readout Order selects whether the signal presented to the ADC is formed by either subtracting the pedestal (stored on pipeline cell 47) from the signal (if the bit set to 1) or by subtracting the signal from the pedestal (bit set to 0). The Ramp Polarity bit controls the direction (positive (0) or negative

(1)) of the ramp generator to correspond to the polarity of the input signal. The third polarity bit, Comparator Polarity, is used to either pass (0) or invert (1) the comparator output so that the signal delivered to the following logic has the same meaning for both positive and negative current input signals. The usual operation for both CDF and D0 has all three polarity bits set to 0.

As shown in Figure 1, the analog comparator feeds a latch and neighbor hit logic. The SVX4 data readout can take one of three different forms depending on the status of two control bits called Read Neighbors and Read All in the neighbor hit logic. If both of these bits are low, the channels to be read out are only those channels (i.e. hit channels) whose digitized outputs exceed the threshold level which was digitally downloaded. If the Read Neighbor bit is set high, then hit channels *and* the channel immediately on each side of the hit channel are also read out. When chips are daisy chained together, neighbor information is passed from one chip to another so that if an end channel is hit, a neighbor channel on the adjacent chip is read out. The readout of neighbor channel amplitudes allows for interpolation to obtain higher hit location accuracy. Under some situations such as testing, all channels on a chip can be read out regardless of signal level by setting the Read All bit high.

The hit threshold level for an SVX4 chip is set digitally and is the same for all channels on that chip. Normally the threshold is set at some fraction of a MIP which results in a relatively coarse threshold resolution (e. g. 2000 e). To overcome this problem, control of the A/D ramp start voltage is provided which allows fine tuning of the noise hit rate. An internal adjustment of the ramp start voltage (RAMP-PED) effectively allows the threshold to be adjusted with 400 e resolution.

The output of the neighbor logic circuit from all the channels form an ordered array of the channels to be read out. Before the chip is read out, the address and data for each channel to be read is stacked in FIFO that uses a token passing system for readout. When readout does begin, channels are read out sequentially beginning with the lowest address channel.. The geographical location of channel 0 is indicated on Figure 1. Since this token passing scheme takes some time readout of a chip in sparse mode with only a few channels at the high end (i.e. near channel 127) having valid signal may fail for the anticipated readout rate; for that reason a Read Channel 63 bit may be set to force readout at this intermediate point and allow for the token ring passing to 'catch-up'. A Read Channel 127 bit is also included for diagnostic purposes.

Control of the SVX4 and data readout is handled by digital and bias pads in the I/O section of the right hand side of the chip. There are three pads called FEMODE, BEMODE, and CHMODE which are used to select one of the four possible operating cycles (Initialize, Acquire, Digitize, and Readout) for the SVX4 when in CDF mode. Sixteen pads, called BUS0-7 and BUS0-7 bar, are used to output address and data information from the SVXII during the Readout Mode. The same sixteen pads are used for real time control of internal switches in the other three operating modes (only for D0 operation, CDF operation was described earlier). For these three modes, the last information on the pads prior to a mode change is held on internal latches before switching to the next mode. Two other pins, Bottom Neighbor and Top Neighbor, are used to communicate with adjacent chips on neighbor readout. Priority In and Priority Out are used to communicate with adjacent chips. These two Priority pins carry different information for each of the four different operating modes.

2 Functional Description

In this Section the function of the SVX4 is described. Section 2.1 gives a brief overview, Section 2.2 describes the operation of the chip in detail, and Section 2.3 gives detailed timing diagrams. Items in the initialization bit stream are described as they relate to operation; a concise list is deferred to

Section 3. Section 2.4 gives the physical layout of the chip, including tables of all the input and output pads. Section 2.5 describes the format for the data output and explains the Gray coding scheme used.

2.1 Overview

The SVX4 consists of 128 identical channels. Each channel has two parts, a Front-End and a Back-End. The Front-End contains the integrator and storage pipeline. The Back-End contains the ADC for digitization and the readout logic and drivers. The major cycles of operation for these parts are Initialization (both), Acquisition (Front-End), Digitization (Back-End), and Readout (Back-End). The initialization cycle usually is performed once, followed by repeated data acquisition, digitization, and readout cycles. The Acquisition cycle occurs simultaneously with the Digitize and Readout cycles in CDF mode, but operated exclusively in D∅ mode. Three input signals, FEMODE, BEMODE, and CHMODE, are used to change the modes as summarized

FE Mode	BE Mode	chip state when in CDF mode	chip state when in D0 mode
0	0	Initialize	Initialize
0	1	--	Acquire
1	0	Acquire & Readout	Readout
1	1	Acquire & Digitize	Digitize

Table 1 Table showing the various states of the chip in either CDF mode or D∅ mode depending on the various conditions of the mode levels (note that these mode levels appear as either inputs on dedicated pads (in CDF mode) or on Bus lines (in D0mode)).

To change the state of the front or back-end, the mode bits are changed, and then the CHMODE pad is pulsed high to complete the transition to the new state of operation. To provide noise immunity and stable operation Mode signals are internally latched on a transparent latch controlled by CHMODE. Thus if CHMODE is low changes in the Mode signals do not change the internal state of the chip; if CHMODE is high the internal state of the chip is determined by the Mode signals Timing specifications and the appropriate levels for FEMODE and BEMODE for each of the three cycles (initialization, acquire, and readout) are given in Section 2.3.

It is also important to realize that depending on which mode (D0 or CDF) has been configured, the bus lines will operate as control for the ADC only (CDF mode) or will operate as control lines for operation in acquire or digitize (D0 mode). The function of the control lines is shown in Table 2. Depending on the mode of the chip, the bus lines could have different functions.

Pin name, Readout mode function	Digitize mode function	Acquire mode function in D0 mode only
Bus0	Comp_rst	--
Bus1	Ramp_rst	--
Bus2	--	PRD2
Bus3	Rref_sel	--
Bus4	--	PARST
Bus5	--	L1A
Bus6	--	PRD1
Bus7	--	CalSR

Table 2 Bus pin multiplexing table. CALSR is ORed with the CALSR pad in the Acquire cycle and ored with WrSEU in the Initialize cycle.

2.2 Detailed Operation

2.2.1 The Front-End

The SVX4 front end was designed at Fermilab and mates with the SVX4 back end, designed at LBL, to produce a complete SVX4 128 channel silicon detector readout chip. The front end contains 128 identical channels of integrating charge preamp and a 46 cell analog pipeline which is cycled by the beam crossing clock. Hit cells are temporarily removed from the pipeline for readout to the back end, where the data is digitized, sparsified, and read out. SVX4 is "dead timeless," so that front end signal acquisition can continue uninterrupted while back end digitization and readout is occurring. Operation of the front end requires only a 2.5V supply, a front end clock, and a few digital control lines. The front end has two modes of operation: **Initialize** and **Acquire**.

In **Initialize** mode, the front end clock signal (FEClk) is routed to control a 148 bit shift register, which is downloaded with program bits. 20 of these bits set programmable parameters such as trigger delay, bandwidth, bias current, etc. The remaining 128 bits form a mask register which is used to selectively enable or disable reception of a calibration test charge to each of the 128 preamp inputs. The serial program bit stream line, Srin, actually comes from the back end chip which also has a programmable register and is a copy of the level presented on PRIN. The serial data is clocked into the registers on the rising edge of FEClk. After downloading of the shift register is complete, application of a strobe pulse (via the CalStrobe control line) transfers the 20 programmable parameter bits to a SEU tolerant shadow register. The strobe also resets the pipeline cell position 0 (i.e. to Cell0). Initialization must be performed after power up and before acquisition begins. Although theoretically not necessary, it may be desirable to periodically repeat initialization to insure that the chip remains in a known operating condition.

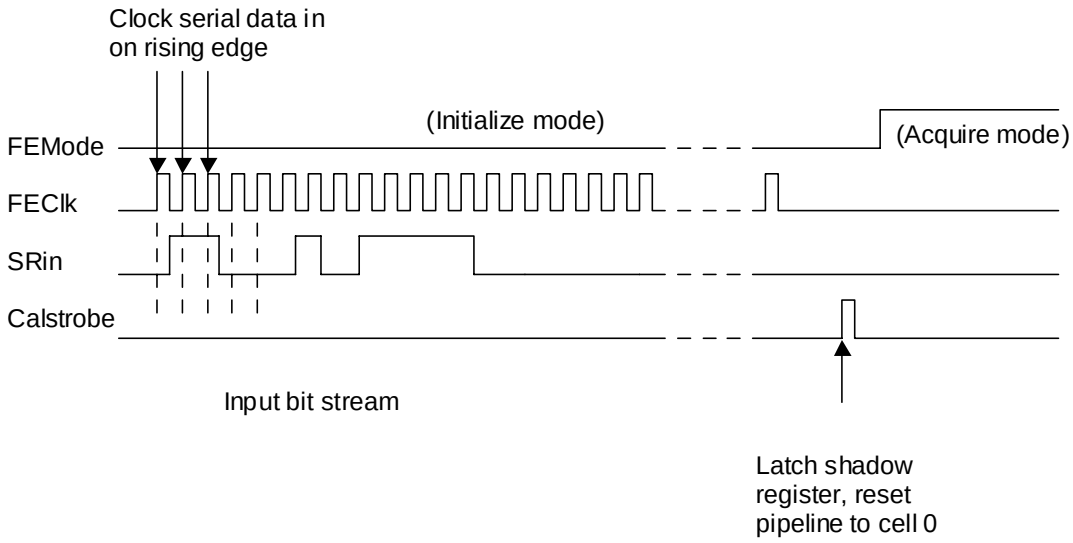

Figure 5 Timing diagram for the initialization of the SVX4.

In **Acquire** mode (see Fig. 5), the front end clock (FEClk) is routed to the analog pipeline and is used to advance the 46 cells in round robin (i.e. circular) fashion at the beam crossing rate. At each of the 128 channel inputs, an integrating charge preamp accepts a positive input charge from the detector, and the preamp output feeds the pipeline. The system charge transfer gain is 15 mV/fC (this is the transfer from input to the SVX4 to the input to the ADC). As the pipeline cells are advanced with the front end clock, they perform correlated double samples on the preamp output, as will be described. A given cell is reset while the front end clock is high, takes a first sample of the preamp output when the clock goes low, and takes the second sample when the clock goes back high, which also advances the pipeline to the next cell. The voltage difference between the two samples, representing the preamp charge integrated during that time, is thus stored in the cell. The duty cycle of the clock obviously controls the amount of time spent resetting and acquiring on a cell. Typically, the front end clock should have a low duty cycle so that only a small portion of the clock cycle time (minimum 20 ns) is spent resetting, and most is used for acquiring the preamp output. This is desirable since the slower the preamp risetime, the lower is its series noise.

Measured PreAmp risetime (in ns, 10% to 90%) vs BW setting and vs Load Capacitance									
BW / Cload	**0**	**1**	**2**	**3**	**4**	**7**	**8**	**11**	**15**
10 pF	**20**	**23**	**27**	**32**	**35**	**46**	**48**	**58**	**64**
33 pF	**38**	**45**	**53**		**65**		**82**		

The dynamic range of the preamp (200 fC) is larger than the dynamic range of the pipeline (40 fC), so that many signal charges can be integrated and sampled without saturating the preamp. However, the

preamp must periodically be reset via an external control line (PreampReset) in order to prevent eventual saturation. PreampReset is active high, with a minimum required width of 80 ns to achieve complete reset. It is typically performed during beam gaps in order to avoid incurring any deadtime. The timing of PreampReset is not critical, but after reset, one beam crossing time (~132 nsec) should be allowed for the preamps to settle before inputs can be accurately acquired.

The Level 1 Accept (L1A) control input is used to remove a "hit" cell from the pipeline, with a delay of from 1 to 42 beam crossings, and temporarily store it in a FIFO so that it is queued for readout to the back end. The delay is determined by the value programmed in the shift register during Initialize mode. L1A is normally high during acquisition, and pulsed low to store a cell. L1A must go low and return high between front end clocks, i.e., while FEClk is low. Up to four cells can be stored in the FIFO and queued for readout. If four cells are stored, additional L1As are simply ignored.

A special pipeline cell, the "pedestal cell," is reserved for acquiring pedestal only. It is used during readout along with a stored cell. The back end essentially digitizes the difference between the hit cell and the pedestal cell. The pedestal cell is not part of the normal round robin of acquisition cells, and so must be explicitly refreshed periodically. This is one of the functions of the PR2 control line. If PR2 is high when FEClk transitions from low to high, then normal acquisition is inhibited for that clock cycle. The normally intended pipeline acquisition cell is skipped over and the pedestal cell instead is placed in the pipeline for acquisition of the pedestal. Thus one cycle of dead time is incurred by refreshing the pedestal cell. If this is done during a beam gap, dead time can be avoided.

Operation of SVX4 is "dead timeless," so that the readout and digitization process can occur in parallel with normal acquisition. Front end cell readout is accomplished by asserting the PR1 control line in conjunction with FEClk (which continues to control normal acquisition). If PR1 is high at the low to high transition of FEClk (PR1 should then subsequently be lowered), the pedestal cell readout is then initiated. The read amp is reset during the first clock cycle, then the pedestal cell is held in the read amp at the start of the second clock cycle. The read amp output feeds the back end, which uses the pedestal voltage to autozero the ADC. When PR1 is raised a second time, the next FEClk low to high transition removes the pedestal cap from the read amp and initiates readout of the stored hit cell, which is read out in a manner similar to the pedestal cell. The hit cell voltage can then be digitized by the back end. If desired, the effective signal polarity which is digitized can be reversed by setting to 1 the Pipeline Readout Order parameter bit in Initialize mode. This reverses the readout order to (signal – pedestal) instead of (pedestal – signal). After digitization is complete, the readout cell needs to be removed from the FIFO and placed back into the pipeline. This is accomplished by doing a PR2, which has the dual function of digitally restoring the cell to the pipeline and of retaking the analog pedestal on the pedestal cell capacitor.

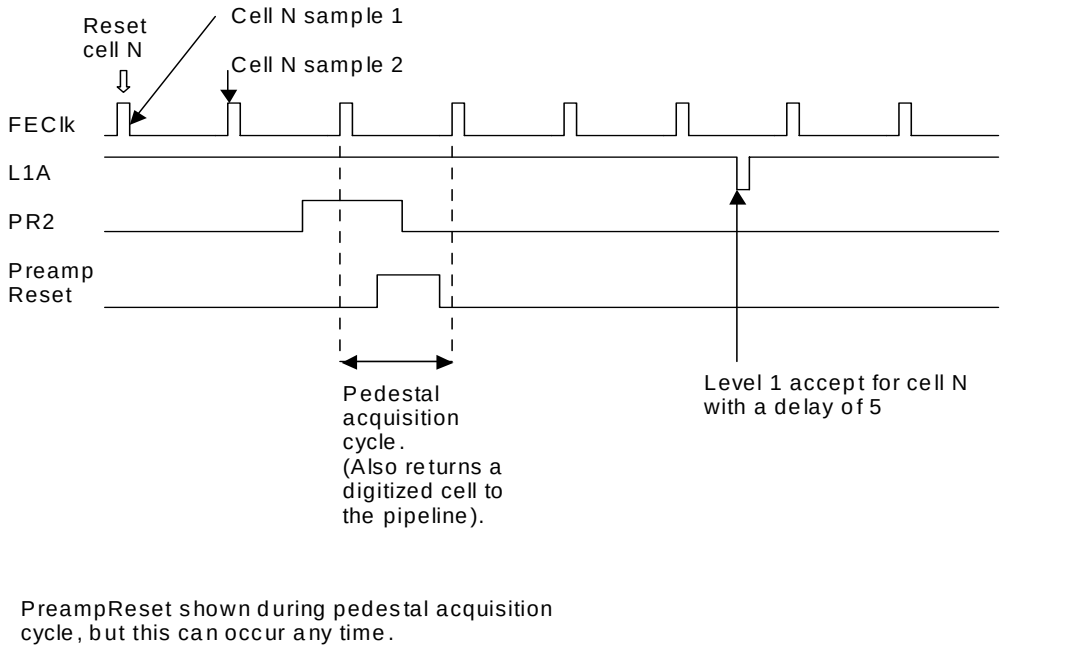

Figure 6 Timing diagram for the acquire cycle of the SVX4.

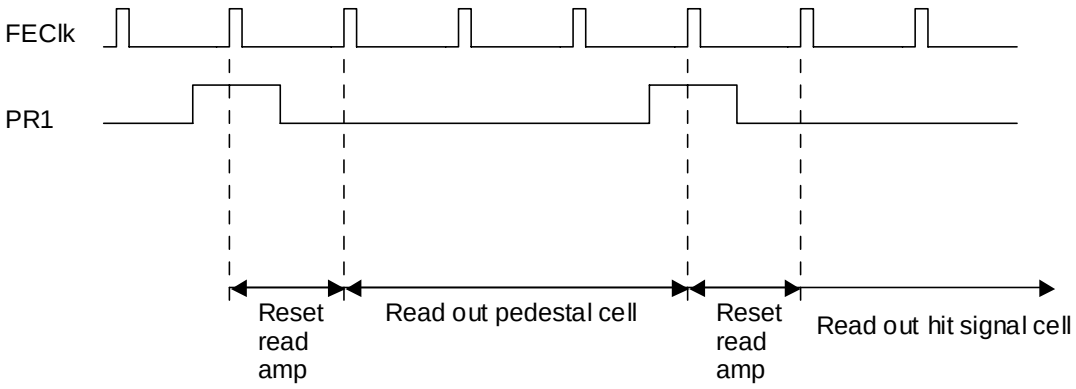

Figure 7 Timing diagram for the pipeline readout of the SVX4.

In order to facilitate testing, a small charge injection capacitor (25 fF) can be switched in from each preamp input to a common bus line. A 128 bit programmable channel register (downloaded in Initialize mode) can function as a mask register, and determines whether or not an injection capacitor is switched in for each channel. When in Acquire mode, the common bus voltage is determined by the state of the CalStrobe control line. When CalStrobe is low, the common bus is grounded. When CalStrobe goes high, the common bus is connected to the VCAL pad. Thus, raising CalStrobe injects a charge of magnitude (VCAL)(25fF) to each channel that has a mask setting of 0.

Usually it is desirable for all channels on a chip to be functional. However, sometimes "black hole" effects (usually due to pin-hole shorts of the coupling capacitors of the silicon strip detectors) are present in detectors, which result in a DC current being applied to a preamp input. This can affect neighboring channels by turning on input diode protection circuits, which can activate parasitic current paths. Therefore, a provision has been included which allows a selected channel's preamp reset to be held high, which harmlessly sinks any positive input current to ground without affecting any other channels. Setting the programmable Mask/Disable bit during Initialize enables this feature. If Mask/Enable is high, then the 128 bit channel register is used not as a charge injection mask register, but as a channel disable register. Any channel that has its mask bit set high will have its preamp reset held always high.

Powering the SVX4 Front End is very straightforward. An analog power supply, **AVDD**, of 2.5V must be provided for the preamp and the analog sections of the pipeline. This supply is bypassed on chip with an integrated 0.012 uF capacitor. Best dead timeless performance is obtained if an external 0.1 uF bypass capacitor is added close to the chip (within an inch or so). The front end analog ground is NOT supplied through a pad, but through the low resistance back side of the die. Thus, the die must be connectively attached to a ground plane. A digital supply (DVDD and DGND) is required to drive the pipeline digital logic. This supply is not derived from front-end pads, but is routed in from the back end chip digital supply. For optimal dead timeless operation, AVDD and DVDD should come from two physically separate power supplies. If, however, front end acquisition will not be occurring simultaneously with back end digitization and readout, it may be possible to derive AVDD and DVDD from the same external power supply.

There is an internal master bias circuit on the front-end chip, which supplies the bias reference for both preamp and pipeline. Preamp and pipeline bias currents can be adjusted via programmable shift register bits. The on-chip bias reference voltage is connected to the **Bias** pad. Under normal conditions, no external bias current reference needs to be provided. Since the bias circuit is referenced to AVDD, an on-chip Bias to AVDD bypass capacitor is included. An external bypass capacitor from Bias to ground can be provided in order to improve the integrator Power Supply Rejection Ratio (PSSR). The optimal value of this bypass will depend on the value of the integrator input capacitance to ground (not to neighbor channels).

Two preamp diagnostic bias pads are included on the prototype so that they can be forced if necessary. (Ncas) supplies an internal preamp cascode voltage, and Vrset controls the placement of the DC reset point of the preamp. Under normal conditions, no connection to these pads is necessary.

Several other diagnostic pads are available for chip testing, including (P127), (R127), and (W127). These are buffered versions of the Ch. 127 preamp output, pipeline read amp output, and pipeline write amp output (see Figure 1 for locations). The buffers are simple PMOS followers that require external bias (a pull-up resistor of 1000 ohms with a 6V voltage has proven adequate). Without an external pull-up, a buffer will be inactive.

2.2.2 The Back-End

The SVX4 back end was designed at LBL and Padova, Italy and mates with the SVX4 front end, designed at Fermilab, to produce a complete SVX4 128 channel silicon detector readout chip. The back end contains 128 identical channels of comparators followed by an analog delay and latch, a common ramp generator for all 128 channels, a specially designed comparator common to all 128 channels used for common mode noise discrimination (also called dynamical pedestal subtraction (DPS), and shown on Figure 7), and a FIFO with control logic for nearest neighbor logic, digital thresholds and sparsification. After a trigger signal or a Level 1 Accept (L1A) is received, every channel is digitized simultaneously, passed through the FIFO control logic, and then read out.

Depending of the mode of the chip, two different actions occur. For the D0 mode, the front end signal acquisition stops while the back end digitizes and readout is completed. For the CDF mode, front end signal acquisition continues simultaneously while digitization and readout is occurring. This "dead timeless operation" therefore requires the use of two independent clocks (FEClk and BEClk) while for D0 mode only one clock is needed (FEClk=BEClk=Clk) that changes frequency accordingly. Operation of the back end requires a 2.5V supply, a back end clock, and a few digital control lines.

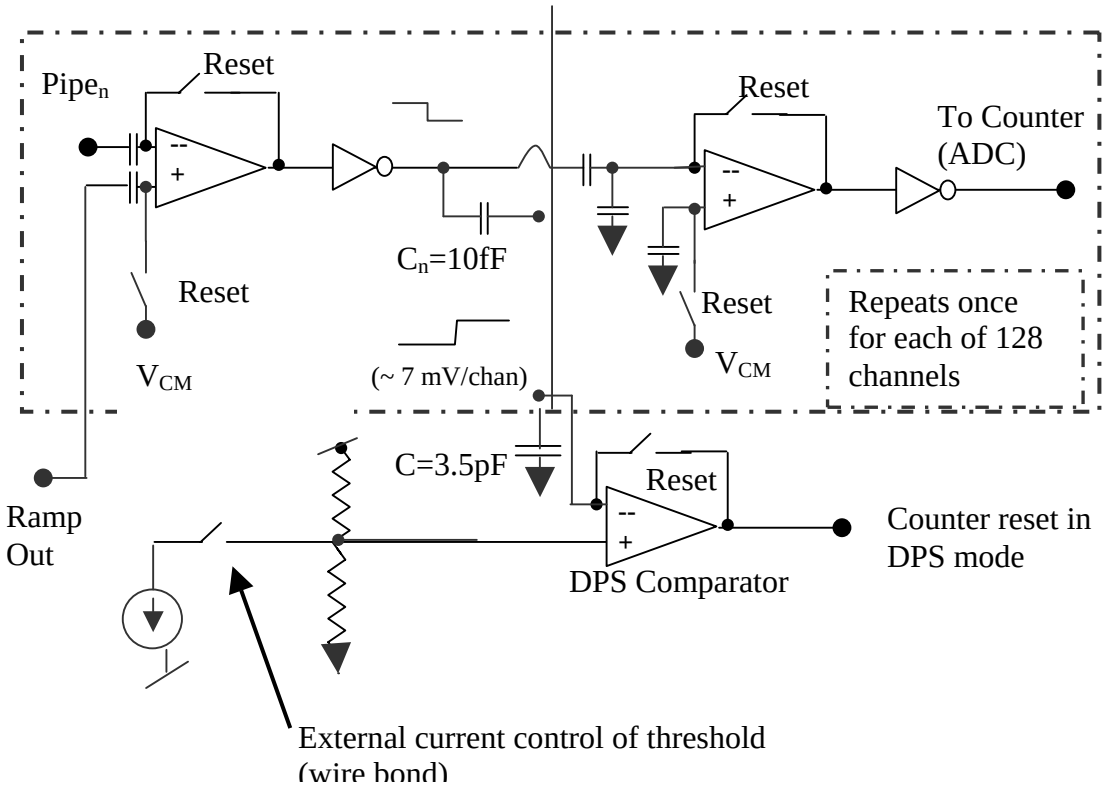

Figure 8: **Dynamic (Real Time) Pedestal Subtraction / ADC Block diagram** – For each channel the selected pipeline cell is compared with the generated ramp which is common to all channels.. The output of the first comparator feeds a second comparator which serves only as a delay circuit. The output of the second comparator is used to latch the Gray counter value and thus provides a measure of the charge on the pipeline capacitor. In addition, the output of the first comparator for all channels are added at the summing junction of the common DPS comparator. When enough channel comparators have fired the DPS comparator fires in turn and releases the Gray counter which until then is continuously reset when the DPS feature is enabled . The number of channels required to fire the DPS can either be determined by an externally supplied bias or via an internal resistor network.

The back end has two cycles of operation: Digitization and Readout.

For completeness, while the chip is in Initialize cycle, the front end clock signal is routed to clock a 46 bit shift register, which is downloaded with program bits from the PRin line. Seven of those bits set the chip ID, 3 bits are used for Vcal switching, 1 bit controls the DPS mode, 4 bits set the digital function of the FIFO, 25 bits set the operation parameters of the ADC, and 5 bits set the driver currents for the SVX4 for OBDV and readout data lines. These bits are transferred to an SEU (Single Event Upset due to the passage of an ionizing particle) tolerant shadow register.

During the Digitize cycle, the back end clock (BEClk) is routed to a counter (nominally during Digitize f = 53 MHz, but since both edges of the clock are used the effective digitization rate is 106 MHz). Proper operation of the ADC is preceded by the manipulation of the ADC control lines. (Note: for D0 mode, the control lines are multiplexed over the bus lines while for CDF mode these control lines are independent of the bus lines.) We show the proper timing of the control lines in Figure 9.

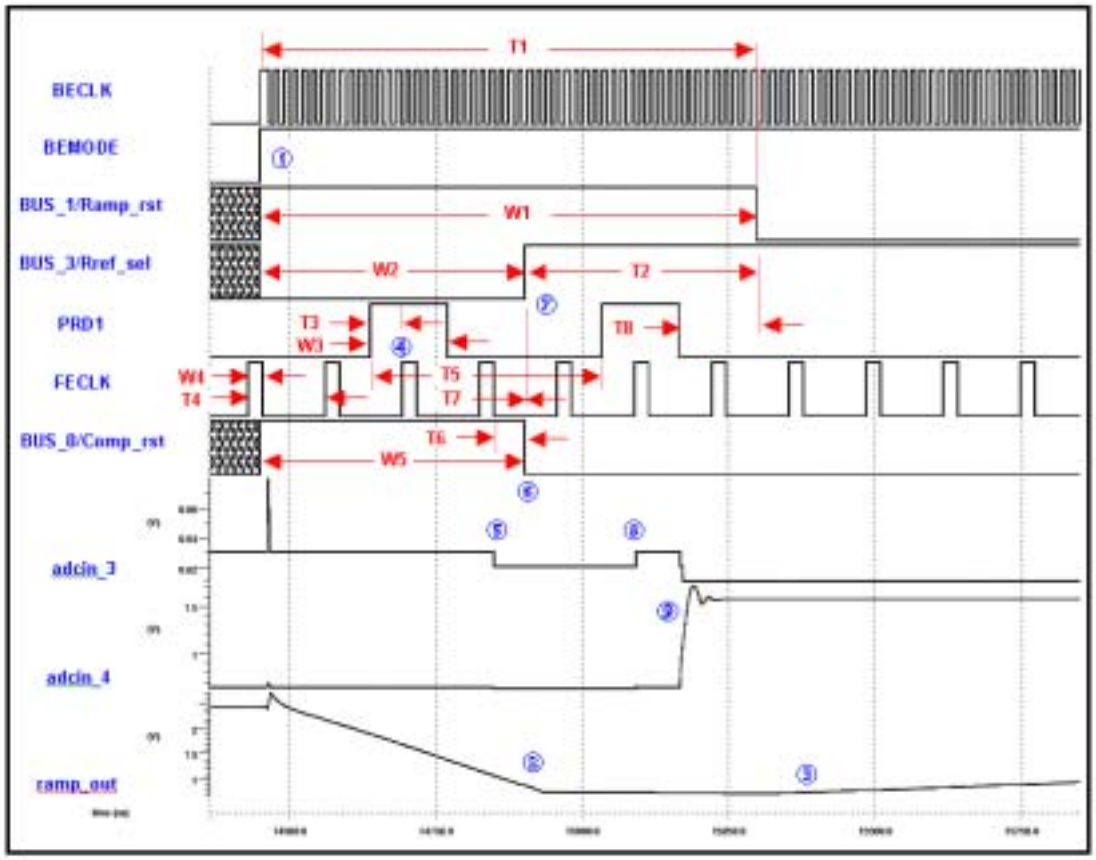

Figure 9 Timing diagram for pipeline read and ADC.

The pipeline read/ADC timing consists of two sets of interdependent signal sequences. One is the *ADC Ramp Setup* (**BECLK/Ramp_rst/Rref_sel**), and the other *Pipeline Read* (**PRD1/FECLK/Comp_rst**).

The *ADC Ramp Setup* controls the ADC ramp generator, the selection of the ADC ramp reference voltage (fixed) or the ADC ramp pedestal (programmable), and start of the ADC counter when not in Real-Time Pedestal Subtraction mode (RTPS). The *Pipeline Read* sequence controls the signal/pedestal CDS of the pipeline read amplifier on one terminal of the ADC input comparator, as well as the ADC ramp sampling on the other. Significant features of the sequences are described below.

ADC Ramp Setup

1) Pipeline read and signal digitization is initiated by entering DIGITIZE mode, that is, by asserting (**FEMODE**=1 + **BEMODE**=1) under **CHMODE**=1 [①]. If **CHMODE** =0, DIGITIZE will instead be entered at ↑**CHMODE** when (**FEMODE** =1 + **BEMODE** =1). This behavior is the result of the MODE pins being processed through a transparent D-latch, which is controlled by **CHMODE**. MODE changes must occur on or about ↑**BECLK**, or while **BECLK**=0. Upon entering DIGITIZE, the I/O pins **BUS_0**, **BUS_1**, **BUS_3**, change function to **Comp_rst, Ramp_rst, RRef_sel,** respectively.
2) Asserting **RRef_sel**=0 while **Ramp_rst** =1 resets the ADC ramp to the fixed ADC ramp reference voltage level [②], which is above the programmable ramp pedestal voltage level. **RRef_sel**=0 while **Ramp_rst** =1 must then be asserted in concert with **Comp_rst**, as described below, in order to subtract the programmed pedestal value from the ramp reference voltage. Asserting **Ramp_rst**=1 also asserts the internal counter reset signal **Cntr_Rst** when RTPS mode is off.
3) When **Ramp_rst** is de-asserted the ADC ramp commences in the programmed direction [③]. If RTPS mode is off, the internal signal **Cntr_Rst** will also be de-asserted. If RTPS mode is selected, **Cntr_Rst** is controlled by the dynamic threshold comparator circuit. In this case, the counter will be held in reset until the dynamic threshold comparator fires, sometime after the ADC ramp is initiated.

Pipeline Read

4) The pipeline signal/pedestal sampling sequence is initiated by ↑**FECLK** under **PRD1**=1. The relationship of **PRD1** and **FECLK** is fixed in terms of the state of **PRD1** during the phases of **FECLK**, as specified above. The 1st ↑**FECLK** under **PRD1** begins the cycle [④]. In the above example, the programmed order ("PB" config bit) is pedestal/signal.
5) During time **adc.T6**, the pipeline pedestal values are sampled onto the ADC input capacitors while the ADC comparator inputs (the other terminal of the input capacitors) are reset to a fixed internal reference level. Concurrently, during time **adc.W5** the ramp reference level is being sampled onto identical comparator input capacitors on the other comparator input terminal. It can be seen on the internal signal **adcin_3** (no-hit channel) that the pipeline pedestal value is available to the ADC at the 2nd ↓**FECLK** [⑤].
6) When **Comp_rst** is de-asserted the ADC comparators are un-reset [⑥]. The ADC input sampling capacitors are now pre-charged to the pipeline pedestal values. From this time on, the ADC input is reading the difference of the pipeline output and the sampled pipeline pedestal, thus the CDS cycle is complete. However, the correct pipeline signal value will not be applied until the 2nd ↓**PRD1**.
7) ↑**RRef_sel** applies the desired offset to the other ADC comparator input capacitor [⑦]. This action must take place after ↓**Comp_rst** (**adc.T7**) in order to achieve the desired CDS operation (rampref-rampped) on the ramp. Note that the effect of this CDS operation is to pre-charge a small offset across the ramp capacitor, which the ramp must "make-up" before it achieves zero-crossing of the original ramp reference level value. The purpose of this process is to allow the ramp to slew for a small period into its linear region, so that the ADC comparators will fire

within the linear region of the ramp for small input signals. This is especially important for accurate noise measurement.

8) On the 3rd ↑**FECLK**, under the 2nd **PRD1**=1, the pipeline pedestal value is de-asserted by the pipeline read amp [⑧]. On the 2nd ↓**PRD1** the signal values are asserted by the pipeline read amp [⑨] {*I am not sure if this is correct—the simulation shows this is the case, but Tom's measurements on the pipeline test chip indicate that it comes on falling FECLK just like the pedestal values—Brad*} . This can be clearly seen on the internal signal **adcin_4** (hit channel) above. Time **adc.T8** is required to allow the pipeline read amp to settle (and hence the signal-pedestal value at the ADC input) before starting the conversion.

Timing Spec	Description	Min	Nom	Max	
adc.T1	1st ↑**BECLK** to ↓**Ramp_rst**	4* **BECLK**	900 nS	--	
adc.W1	Width of **Ramp_rst** in DIGITIZE mode	600 nS	900 nS	--	
adc.W2	Width of **RRef_sel** low under **Ramp_rst**	500 nS	600 nS	--	
adc.T2	↑**RRef_sel** to ↓**Ramp_rst**	200 nS	300 nS	--	
adc.T3	↑**PRD1** to 1st ↑**FECLK** of pipeline read	5 nS	54 nS	--	
adc.W3	Width of a **PRD1**	30 nS	1* **FECLK**	--	
adc.W4	Width of **FECLK** high	20 nS	25 nS	--	**
adc.T4	Period of **FECLK**	65 nS	132 nS	--	
adc.T5	Time between two ↑**PRD1** for pipeline read	3* **FECLK**	4* **FECLK**	--	
adc.T6	2nd ↓**FECLK** of pipeline read to ↓**Comp_rst**	55 nS	132 nS	--	
adc.T7	↓**Comp_rst** to ↑**RRef_sel**	50 nS	50 nS	--	**
adc.W5	Width of **Comp_rst**	100 nS	455 nS	--	
adc.T8	2nd ↓**PRD1** to ↓**Ramp_rst**	100 nS	132 nS	--	

Table 3 Timing for the various signals for pipeline readout and ADC setup. Items marked by ** are critical for proper operation of the SVX4.

9) The slope of the ramp is determined by the value of the external resistor connected to the ISLOPE pad and the values of the RampRng control variable. For the nominal external resistor of 36 kohm and with RampRng = 0 this is 0.5 mV/nsec. This sets the sensitivity of the ADC, i.e. number of ADC counts per electron. Though the operating frequency of the back end clock during digitization is set to 106 MHz, this frequency can be altered and therefore the number of ADC counts per electron is altered as well. Approximately, the conversion is for read all mode

ADC counts = ADC delay / 2 * f(BEClk) + pedestal / 2 * f(BEClk)
+ (Q * 15 mV/fC) / Ramp Rate (R ext) / 2 * f(BEClk)

and the conversion for DPS mode is

ADC counts = ADC delay / 2 * f(BEClk)
+ (Num of e's / C) / Ramp Rate (R ext) / 2 * f(BEClk)

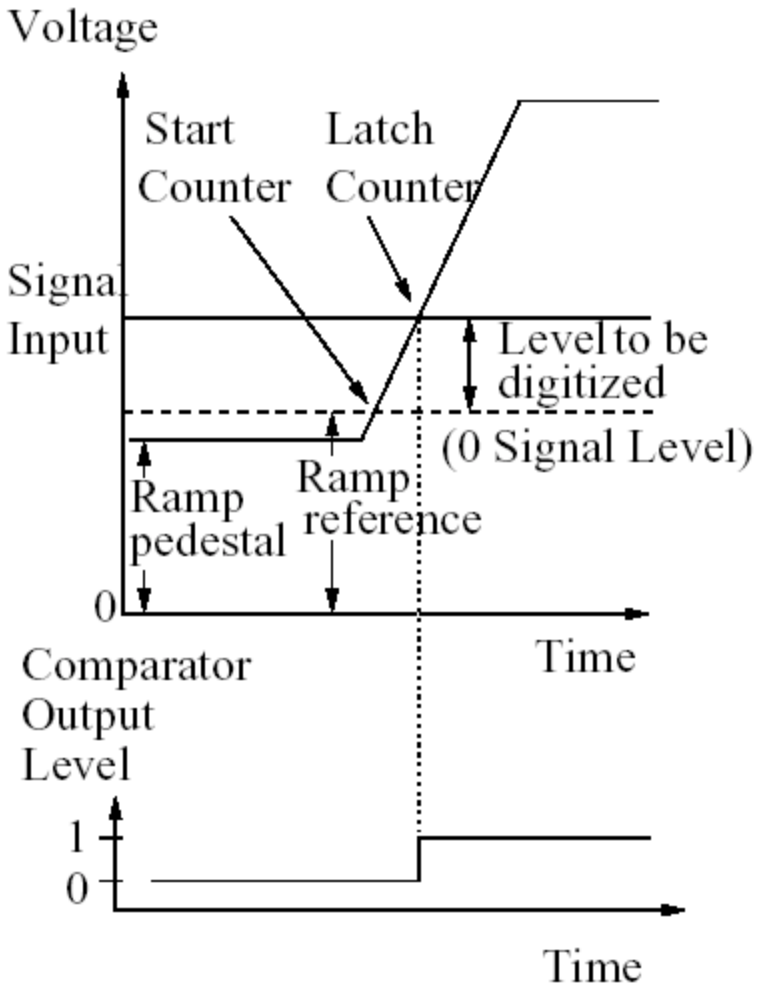

Figure 10 Comparator operation for the default polarity (000). Ramp reference is set either externally or via an internal volatage source.

If sparsification is on, the digital threshold that is downloaded to the chip is used as a semaphore to tag the channels for readout.

In Readout Cycle, the FIFO drops a token which is systematically passed to each individual channel sequentially. A channel is flagged for readout if the value stored during Digitize is over the threshold value, or Read Neighbor is set and the neighbor value is over the digital threshold, or Read All is set or Read Channel 63 or Read Channel 127 are set. Timing considerations as outlined in section 1.3 force us to read channel 63 at all times

3 The Difference Between D0 and CDF Modes

The SVX4 has the ability to operate in two modes: D0 mode and CDF mode. What does that mean?

Physically, there is an external pad on the chip that must be wirebonded to AVDD/DVDD or GND. If this pad is not bonded correctly, there is no guarantee the chip will function properly (even though the level is pulled weakly to GND – i.e. to CDF mode). If the chip is bonded to AVDD/DVDD the chip will operate in D0 mode. When the chip is in D0 mode, it does not have the ability to acquire data while digitizing or readout. Internal to the chip , this means that the front end clock is not gated when the chip is in readout mode. It is necessary only to drive the front end clock during initialize and acquire. During digitize only the back end clock is needed and similarly for readout. All 46 pipeline cells are available, but there is no secondary pipeline to store events. D0 necessarily wirebonds the front end and back end clocks together meaning there is only one clock in the system.

If this pad is grounded, then the chip is in CDF mode. This means that the chip can acquire data and digitize simultaneously. In order to have this functionality requires the use of two independent clocks. Physically, this means the back end clock maybe operating while the front end clock is running at a different frequency. The pattern for setting up the ADC is similar, but the control signals are transmitted differently.

In D0 mode, the control lines for PRD1, PRD2, L1A, CALSR, RMPRST, RREFSEL, and COMPRST are multiplexed over the differential bus lines. In CDF mode, the control signals PRD1, PRD2, L1A, and CALSR are transmitted through independent control lines, while the RMPRST, RREFSEL, and COMPRST are multiplexed over the bus lines identical to D0 mode. By correctly wirebonding the D0 mode pad , a latch inside the chip is set that determines where the control signals will be taken from.

It should be noted that the chip has been operated successfully in a hybrid mode – i.e. in a two buffer mode. In such a case the D0/CDF wire bond pad was controlled externally, i.e. the chip could be put in either mode on the fly. Both front end and back end clocks were provided. The chip was set to CDF mode and data was acquired in the usual fashion. by the front end clock. When a trigger occurred, the external sequencer switched to D0 mode, issued L1 accept and two PRD1 signals to set up the chip to readout the first capacitor and then switched back to CDF mode. Digitize and readout worked as they during normal operation. If another L1 trigger occurred during digitize and read out, the front end clock halted to preserve the L1 data and raise L1busy to stop additional triggers. After completing readout, the sequencer switched back to D0 mode and issue a PRD2. If there was a pending trigger, it would follow with 2 PRD1's to set up to digitize the signal.

4 Initialization Bit Stream

SVX4 Configuration Register Table

Bit Number	Bit Name	Description	Values	Nominal Setting
— Front end Bit Assignments —				
0:127	Mask [127:0]	Cal mask or channel disable register (see bit 130 for assignment)	0 = mask/enable 1= unmask/disable	0 .. 0
128	spare	spare	X	X
129	VCAL	Connects the VCAL pad to the internal voltage divider	0=not connected to pad 1=connected to pad	1
130	Disable	Select whether mask reg acts as a channel disable reg or a cal mask reg	0 = cal mask 1= channel disable	0
131:134	BW [0:3]	Preamp rise time adjustment (depends on input capacitance), binary weighted	For Cin=10 pF: Tr ≈ 25 nS + (BW * 4 nS) For Cin=50 pF: Tr ≈ 60 nS + (BW * 10 nS)	0010
135:138	Isel [0:3]	Preamp input FET bias current adjustment, binary weighted	Bias current ≈ 164 uA + (Isel * 32 uA)	0010
139:140	IWsel [0:1]	Pipeline write amp bias current adjustment, NOT binary weighted	Bias current ≈ 26 uA + (IWsel0 * 26 uA) + (IWsel1 * 26 uA)	10
141:142	IRsel [0:1]	Pipeline read amp bias current adjustment, binary weighted	Bias current ≈ 26 uA + (IRsel * 13 uA)	10
143:148	PickDel [0:5]	Trigger latency; select system L1A delay as a number of FEClk periods	0 .. 42	TBD
149	PB	Pipeline readout order	0 = pedestal, signal 1 = signal, pedestal	0
— Back end Bit Assignments —				
150:156	ID [6:0]	Chip ID assignment	0 .. 127	TBD
157	RTPS	Real Time Pedestal Subtraction disable	0 = RTPS on 1 = RTPS off	0
158	Rd127	Always readout channel 127 regardless of hit status	0=Rd127 off 1 = Rd127 on	0
159	Rd63	Always readout channel 63 regardless of hit status	0=Rd63 off 1 = Rd63 on	0
160	RdAll	Always readout all channels	0=RdAll off 1 = RdAll on	0
161	RdNeigh	Readout hit channels and their neighbors	0=RdNeigh off 1 = RdNeigh on	1

Bit Number	Bit Name	Description	Values	Nominal Setting
162:165	RampPed [0:3]	ADC ramp pedestal setting, binary weighted	RampDir=0: Ped ≈ 480 mV +(RampPed * 23 mV) RampDir=1: Ped ≈ 1.8 V -(RampPed * 23 mV)	0001
166	RampDir	ADC ramp direction, ramp up or ramp down	0 = ramp up 1 = ramp down	0
167	CompPol	Comparator polarity; sets comparator and delay input for 0→1 or 1→0 transition	0 = 0→1 (for RampDir=0) 1 = 1→0 (for RampDir=1)	0
168:170	RampRng [0:2]	ADC ramp range, adjusts slope of ramp	Slope ≈ 0.5 mV/nS * $[1+(2*r0)+(2*r1)+(1*r2)]^{-1}$	000
171:178	Thresh [7:0]	ADC digital threshold setting, Gray code	0 .. 255	TBD
179:186	CntrMod [7:0]	Counter Modulo, sets counter value at which overflow occurs, Gray code	0 .. 255	TBD
187	FC	First Chip flag; enables the first chip to drive OBDV before readout begins	1 = this is the first chip	0
188	LC	Last Chip flag; enables the last chip to drive OBDV after readout ends	1 = this is the last chip	0
189:191	DriverI [2:0]	Output driver current select; selects output series resistance; the resistance selected appears in series on EACH output pin (plus and minus)	$R \approx [(d2/43) + (d1/86) + (d0/172)]^{-1}$ Drivers off if DriverI = 0	111

Notes:
1) The correspondence of the bus notation indicies are preserved in the table above from column-to-column, i.e. for "Bit Number 162:165," RampPed [3] corresponds to Bit 165, which corresponds to a "1" in the "Nominal Setting" column. This correspondence explicitly determines whether the LSB or MSB of a bus loads first, since there is no common rule.

2) The "Bit Number" references under "Frontend Configuration Register Bit Assignments" are reversed with respect to the "SVX4 Front End" document, in order to accommodate a contiguous, ascending bit order for the complete configuration register.

3) Bit 0 loads first.

4) Vped = Vref - (11 - setting) * 23mV. This actually holds for settings from 0 to 14. When going from 14 to 15, the step is 6 times the nominal step, or 138 mV.For a positive going ramp, we want Vref to be lower than Vped so that the ramp must go for a while before flipping the comparator, thus we normally use settings less than 11. Settings greater than 11 would be used for opposite polarity operation. 11 is the "zero" setting, and theoretically the measured pedestal for this setting would just give the (comparator delay + analog delay), which nominally in simulation for versB is 120 ns. At 10ns/count this would give 12 counts.

4.1 SVX4 Configuration Register Explanation

Below we give an extended discussion of the bits that are downloaded into the configuration register.

0: PB (pipeline readout polarity bit). 0 = pedestal – signal, 1 = signal – pedestal.

1-6: Pipeline level 1 trigger delay. Bit 1 is MSB, bit 6 is LSB. Valid range is 1-42.

7-8: IRSel1-0 (pipeline read amp bias current select). Read amp bias current = 13 uA + (IRSel0)*(13 uA) + (IRSel1)*(26 uA). Increasing the read amp bias current simply speeds up the risetime. The lowest current is probably acceptable.

9-10: IWSel1-0 (pipeline write amp bias current select). Write amp bias current = 26 uA + (IRSel0)*(26 uA) + (IRSel1)*(26 uA). Increasing the write amp bias current speeds up the pipeline reset speed and the pipeline risetime. Nominal bias current = 52 uA.

11-14: Isel3-0 (preamp input transistor bias current select). Bias current = 164 uA + (Isel3)*(256 uA) + (Isel2)*(128 uA) + (Isel1)*(64 uA) + (Isel0)*(32 uA).

15-18: BW3-0 (preamp bandwidth). Used to adjust preamp risetime. Risetime will depend on input capacitance, bias current, and bandwidth setting. The bits are binary weighted: BW0 = LSB, BW3 = MSB.

19: Mask/Disable. If Mask/Disable = low, then the 128 bit channel register functions as a mask register for test charge injection (register bit = high to enable charge injection). If Mask/Disable = high, then the 128 bit channel register functions as a channel disable register (register bit = high to disable channel).

20-147: Channel register <0:127>

4.2 The Output Data Format for the SVX4

The SVX4 generates an 8-bit (byte) output on the 8 differential data bus lines (numbered as BUS0 to BUS7 or DATA0 to DATA7 and their differential complements, 0 being least significant bit) on every transition of the OBDV, the positive side of the differential Output Data Valid signal level. Thus data is presented on both positive-to-negative and negative-to-positive transitions of OBDV. The edges of the transitions of the BUS lines and OBDV are simultaneous at the output of the SVX4 chip; it is left for the readout electronics to generate the appropriate delay on OBDV and properly strobe the BUS lines. The Chip ID byte appears on the first negative-to-positive OBDV transition. The Pipeline Id appears on the first positive-to-negative transition of OBDV.

The output stream is of variable depth depending on many parameters (e.g. threshold, read all, read neighbor, read 64, etc.) and on the amount of true data (or noise!) seen at the input of the SVX4. As long as valid data is being generated by a chip the PRIOUT is asserted high, and a chip will assert PRIOUT and generate data on the BUS lines and toggle OBDV only if the PRIIN is low; PRIIN is weakly pulled to low via an internal resistor. These assignments allow for the daisy-chained readout described in more detail in Section 5. Finally it should be noted that OBDV is nothing more but an

appropriately regenerated and delayed form of the BECLOCK, which is used to clock the data on the output BUS lines.

Output Stream Format :

Byte no	Content	Comments
1	Chip ID	Has highest bit set to 1, the rest are derived from the downloaded parameters (i.e. lowest value in Hex is "80")
2	Pipeline Cell Number	True (physical) number of cell being digitized Can be 1 to 42 decimal (but not 0), the two most significant bits are always 0.
3	Channel Id	Can be 0 to 7F hex (127 decimal), increasing.
4	Data for above Channel Id	Gray Coded (0 to 255 decimal)
…	…	
Last-1	Channel Id	Can be 0 to FE hex (127 decimal), increasing.
Last	Data for Above Channel Id	Gray Coded (0 to 255 decimal)

Thus the minimal readout is 2 bytes (Chip ID and Pipeline Cell) and no data, presumably due to no channel being above pedestal, and also due to Read All, Read 127, and Read 63 bits being off as well.

4.2.1 Gray Code information

Algorithm for Binary to Gray conversion

binary = $B_j\ B_{j-1}\ \ldots\ B_1\ B_0$

gray = $G_j\ G_{j-1}\ \ldots\ G_1\ G_0$

$G_j = B_j$, and G_i = XOR (B_{i-1}, B_i)

B_i are the binary digits, i= 0 to j

G_i are the digits of Gray coded number

Note: 0 is the least significant bit and j is the most significant bit

Algorithm for Gray to Binary conversion

defined in a recursive fashion only

$B_j = G_j$, and B_i = XOR (G_i, B_{i+1})

Note: j here is the most significant bit and one works towards the least significant bit

The embedded MS Excel Spreadsheet allows for an easy translation between the codes, alternatively one can go to the Appendix for the same information.

RED numbers are input

Use the next four lines to convert between decimal, hex , and binary

Decimal	Hex	Binary
111	6F	1101111
110	6E	1101110
109	6D	1101101

Now insert the value aobtained above into the appropriate "NORMAL" cells in the lines below

	NORMAL decimal	Hex	binary	GRAY bits	"hex"	"decimal"
normal=>gray	108	6C	1101100	1011010	5A	90
gray=>normal	90	5A	1011010	1101100	6C	108

	GRAY "decimal"	"hex"	bits	NORMAL decimal	Hex	binary
gray=>normal	94	5E	1011110	1101011	6B	107
normal=>gray	107	6B	1101011	1011110	5E	94

5 Mechanical and Electrical Specifications

We went through and measure all the specifications of the SVX4 chip and they are listed below. Various data was collected by the designers of the chip and that data is listed in tabular format.

5.1 Pad layout

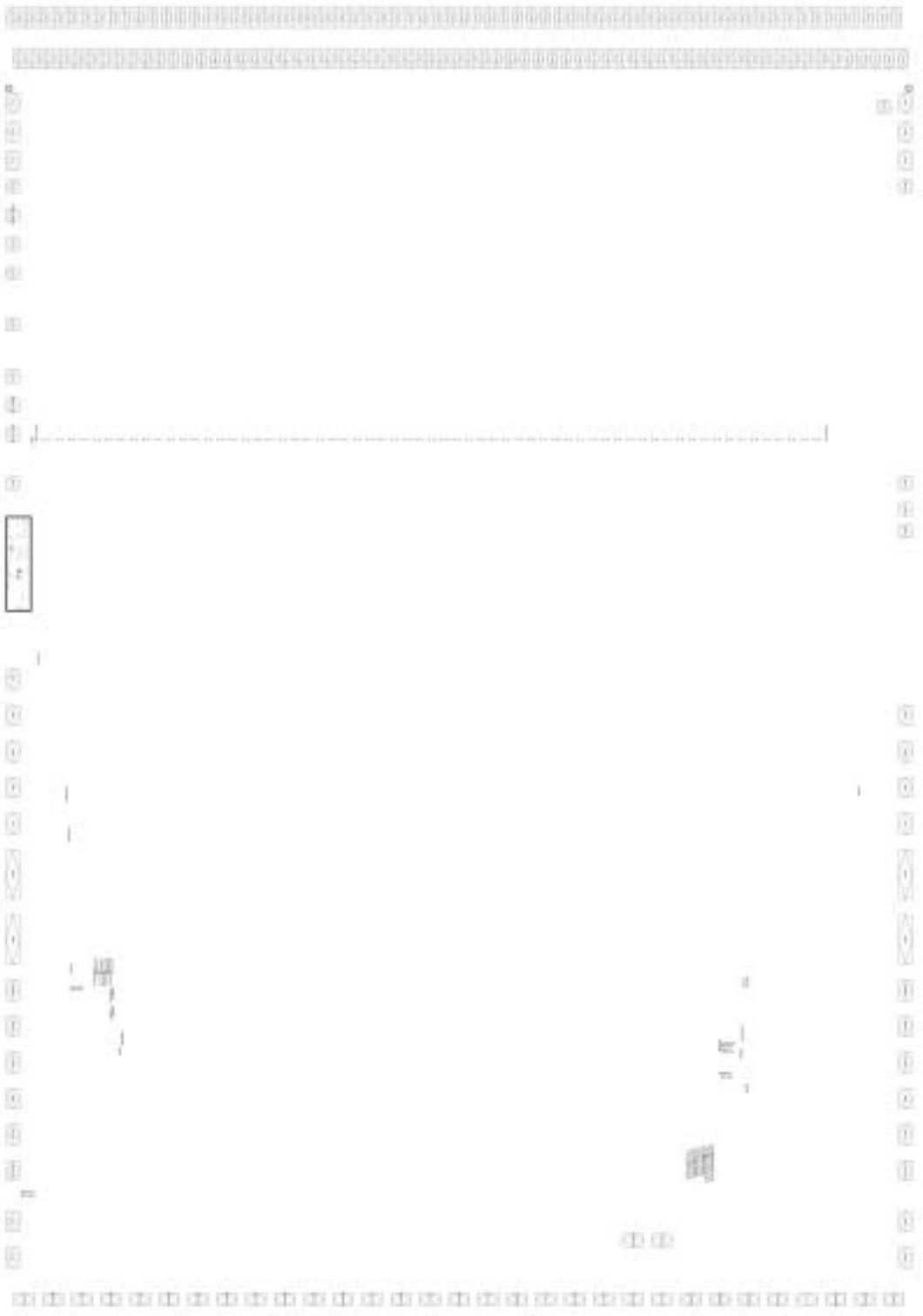

Figure 11 Pad layout on the SVX4

Click here to get a PDF file that you can expand easily

5.2 Pin List for the SVX4

Pin Number	Pin Name	Type Analog Digital	Type Input Output	Nom. Voltage	Wire Bonded	Description & External Components Required
1, 79	VCAL	A	I	AVDDfe ÷ 4	Either	Calibration charge setting
2, 15, 71, 78	AVDD	A	I	2.5	Either	Analog power supply—decouple to gnd! w/0.1 uF
3, 77	Bias	A	I	0.8	Either	Frontend master bias reference—decouple to AVDDfe w/10 nF
4, 76	VRset	A	I	1.0	No	Frontend reset level reference voltage
5	PreampBuf127	A	O	--	No	Ch127 preamp buffered output; requires ext resistor
6	Ncas	A	O	0.6	No	
7, 8, 9, 12, 13, 75, 210	gnd!	A	I	0	No	Analog ground, substrate
10	ReadBuf127	A	O	--	No	Ch127 Pipeline Read amplifier output; requires ext. resistor
11	WriteBuf127	A	O	--	No	Ch127 Pipeline Write amplifier output; requires external resistor
14, 72	AREF	A	I	2.5	Either	ADC ramp pedestal DAC reference
16, 70	IQUI	A	I	0.6	Either	ADC and data receiver bias current setting—7.7k resistor to AVDDadc
17, 69	VTH	A	I	0.9	Either	Dynamic Pedestal Subtraction threshold voltage setting
18, 68, 74	gndd!	A	I	0	Either 19 or 69	Digital ground
19, 67, 73	vddd!	A	I	2.5	Either 20 or 68	Digital Vdd
20, 66	D0MODE	D	I	0/2.5	Either	Connect to vddd! for D0, gndd! For CDF mode
21, 65	USESEU	D	I	0/2.5	Either	Connect to vddd! to select SEU register for configuration, or gndd! for shift register output

Pin Number	Pin Name	Analog Digital Diff	Input *Output* I/O	Nom. Voltage	Wire Bonded	Description & External Components Required
22, 64	ISLOPE	A	I	1.5	Either	ADC ramp slope bias—36k resistor to gnd!
23	BNBR	D	I/O	0/2.5	Yes	Bottom Neighbor; open drain w/2k internal pull-up
24	PRIOUT	Diff	O	0-2.5	Yes	Priority Out plus
25	PRIOUTB	Diff	O	0-2.5	Yes	Priority Out minus
26, 60	SVDD	A	I	2.5	Either	Output Driver supply
27, 59	SGND	A	I	0	Either	Output Driver ground
28	EXTRA	--	--	--	No	Spare pad
29, 31, 33, 35, 37, 39, 41, 43	BUSB<7>, .., BUSB<0>	Diff	I/O	0-2.5	Yes	Data bus 7—0 minus (see "Bus Pin Multiplexing Table" for secondary pin function by mode)
30, 32, 34, 36, 38, 40, 42, 44	BUS<7>, .., BUS<0>	Diff	I/O	0-2.5	Yes	Data bus 7—0 plus (see "Bus Pin Multiplexing Table" for secondary pin function by mode)
45	OBDVB	Diff	I/O	0-2.5	Yes	Odd Byte Data Valid minus
46	OBDV	Diff	I/O	0-2.5	Yes	Odd Byte Data Valid plus
47, 208	BECLKB	Diff	I	0-2.5	Either	Backend Clock minus
48, 209	BECLK	Diff	I	0-2.5	Either	Backend Clock plus
49	FECLKB	Diff	I	0-2.5	Either	Frontend Clock minus
50	FECLK	Diff	I	0-2.5	Either	Frontend Clock plus
51	CHMODE	D	I	0/2.5	Yes	Change Mode
52	BEMODE	D	I	0/2.5	Yes	Backend Mode (Mode 1)
53	FEMODE	D	I	0/2.5	Yes	Frontend Mode (Mode 0)
54	CALSR	D	I	0/2.5	Yes*	Cal Strobe (Acquire mode) Write SEU reg (Initialize)
55	L1A	D	I	0/2.5	Yes*	Level 1 Accept
56	PIPERD2	D	I	0/2.5	Yes*	Pipeline Read 2
57	PIPERD1	D	I	0/2.5	Yes*	Pipeline Read 1
58	PARST	D	I	0/2.5	Yes*	Preamp Reset
61	PRIINB	Diff	O	0-2.5	Yes	Priority In minus
62	PRIIN	Diff	O	0-2.5	Yes	Priority In plus
63	TNBR	D	I/O	0/2.5	Yes	Top Neighbor; open drain w/2k internal pull-up
80-207	In<0—127>	A	I	0.45	Yes	Detector Inputs

The differential signals are LVDS - i.e. they are signals designed to be driven over a differential line of a characteristic impedance of 100 ohms and must be terminated into 100 ohms. The voltage differential is nominally 350 mV, and the mean voltage is 1.25V (i.e. the single ended voltage in the ideal situation should vary from 1.075 volts to 1.425 volts). LVDS signals can tolerate significant common mode noise (0<Vsingle<2.5V).

Power consumption is described in detail in the tests document (as of now it is a draft).

Operating Voltage:	2.5 V nom., 2.25 V min., 2.7 Vmax., all supplies
Absolute Max. Voltage:	3.5 V all supplies*
Operating Current: AVDD:	60 mA
SVDD:	22-160 mA Readout mode
DVDD:	20 mA Readout mode (readall) or 9.2 mA Digitize mode, plus 30mA Acquire mode
Operating Frequency:	FECLK: 7.6 MHz @ 20% duty cycle BECLK: 25 MHz Readout mode, 56 MHz Digitize mode @ 40-50% duty cycle
ESD protection:	for detector input pads, diode protection to AVDD/AGND; for all other pads, diode protection to xVDD/AGND with active power supply clamps to AGND

* Could cause permanent analog performance degradation. TBD.

5.2.1 A note regarding Vcal

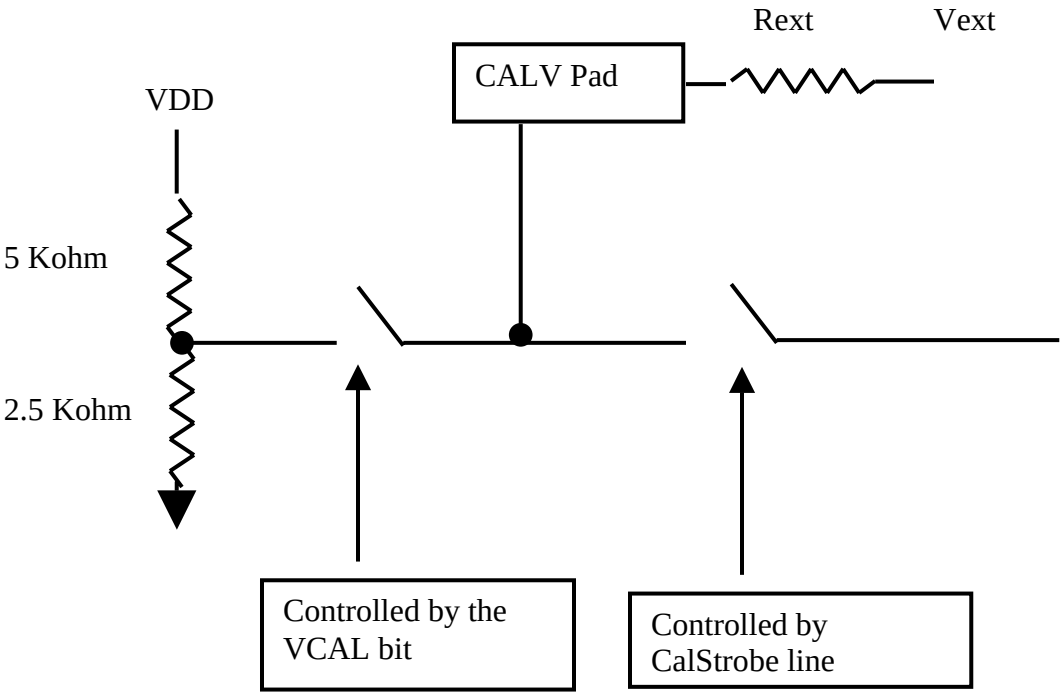

Figure 12

The voltage used to pulse the Cal Inject capacitors is derived either from the voltage applied to the CALV pad or from an internal voltage divider as shown in the above figure. This arrangement, in the case of a multiplet of SVX4 chips supplied from a common external voltage via a shared resistor (Rext), allows for a 'poor mans way' of generating a variety of calibration voltages by turning on and off the VCAL bits for some of the SVX4 chips without the use of a variable external voltage !

5.3 External Components and Power <modify/remove>

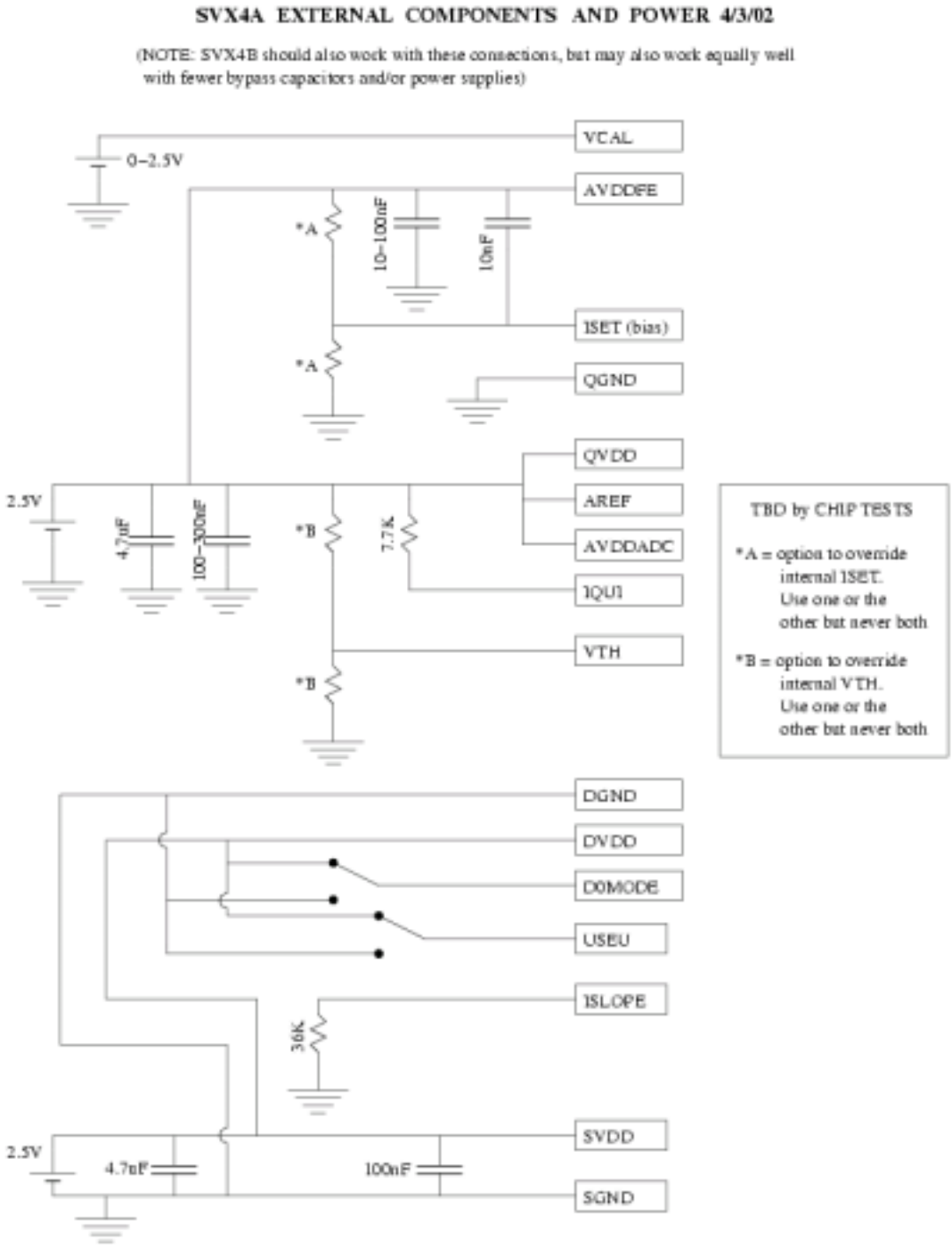

Figure 13 Diagram showing the external components that are needed for proper operation of the SVX4 chip.

6 Operating the Chip

The SVX4 chip is a monolithic chip incorporating a "front-end" section and a "basic-end". In earlier versions these were on separate chips, and it is still common practice to refer to the "front-end" and "back-end" areas. Thus, the following nomenclature is used:

- BE → "BE" is for "back-end". This area has the digitization, FIFO and readout logic.
- FE → "FE" is for "front-end". This area has the analog amplifier, pipeline, and deadtimeless skip-logic
- Hybrid → the ceramic circuit layout that holds 2 to 10 SVX4 chips and services either r-ϕ side of the r-z side of the silicon sensors.

6.1 Guide for Single Chip Operation

- Ideally there should be one very large bypass capacitor (greater the 1 μF) per hybrid for AVDD and DVDD.
- There should be one common ground plane for the chip sets on the hybrid. An exposed section of this ground plane is where the back face of the SVX4 chip rests. The digital power feed should have its own return line, connected to the ground plane at one point per hybrid.
- IQUISCIENT should be biased with a 7.7 kΩ resistor to AVDD. ISLOPE should be biased with a kΩ resistor.
- FECLK and BECLK should be wired bonded together.

6.2 Guide for Daisy Chain Operation

The SVX4 is designed for daisy chained operation to minimize the number of bus and control lines required to operate the device. Fewer control lines means less space on the high density interconnect and less mass in the system. A group of daisy chained chips is shown in Figure 14. All the chips share a common communication bus (BUS0-7) and a common differential clock (FE-CLK, BE-CLK).

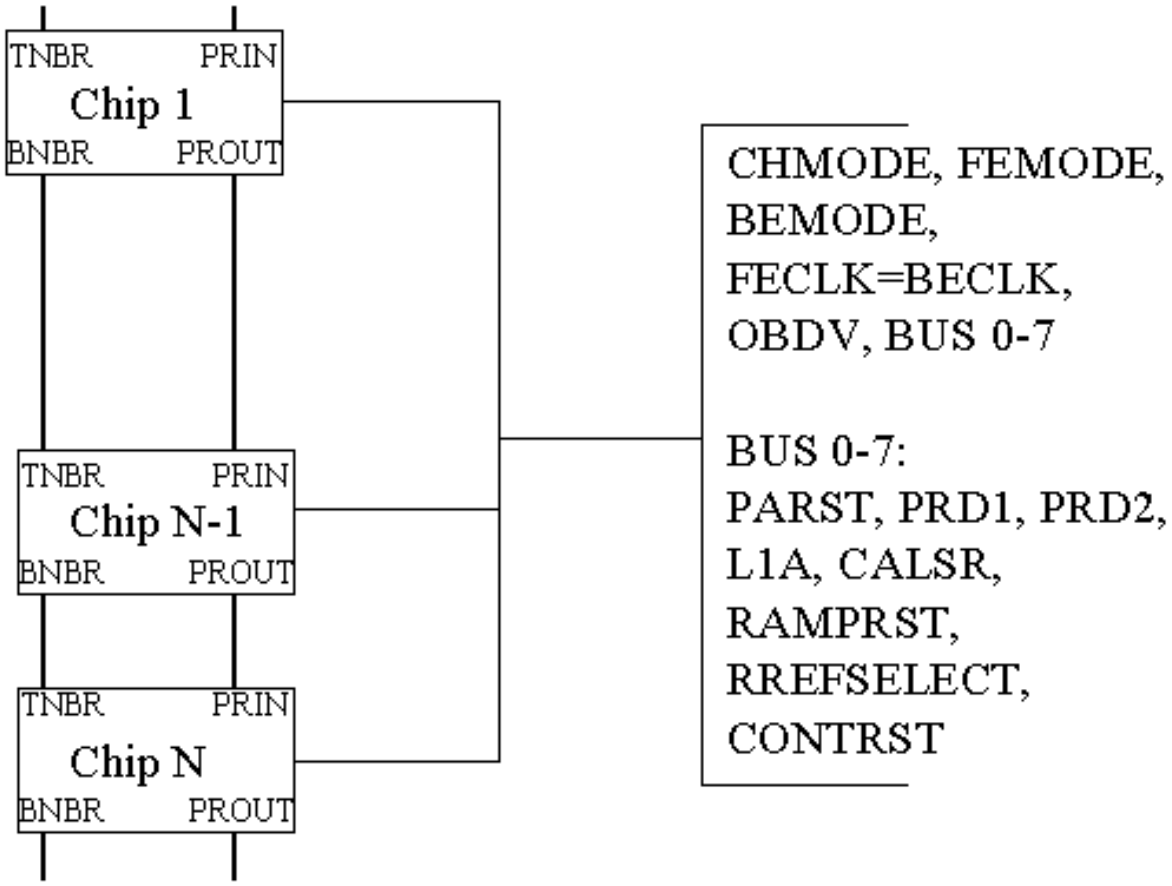

Figure 14 Daisy chained readout chips.

In addition, each chip has two pads call TNBR and BNBR which are used for communication between adjoining chips. After powering up the SVX4, the chip parameters listed in Section 3 must be downloaded before useful operation of the readout chips can begin. For each SVX4 chip, 198 bits must be downloaded into internal registers. In the Initialization Cycle, the signal lines PRIIN and PRIOUT are used as a serial data link to form a very long shift register for downloading parameters to the string of daisy chained SVX4s. Parameters for each chips are loaded in sequential order with the data for chip 1 loaded first via PRIOUT on the last chip of the daisy chain. Data is clocked between cells in the shift register using the common differential clock pads. If there were 10 chips, exactly 1980 bits would have to be downloaded in the Initialize Cycle. Downloaded parameters may be checked by shifting the bits out through PRIIN of the first chip while reloading the chips with the same data. To identify each chip in the daisy chain, a separate chip ID number (bits -) is downloaded into each chip during the Initialize Cycle. The seven bit chip ID number allows chips to be tagged with numbers from 0 to 127.

In Acquire Cycle, the Bus 0-7 and clock pads provide simultaneous real time control of all the chips in the daisy chain. PRININ, PRIOUT, TNBR, and BNBR have no function in Acquire Cycle.

In Digitize Cycle, the Bus –0-7 and differential clock pads provide real time control of all the chips in the daisy chain. The TNBR and BNBR pads are used only in READ NEIGHBOR mode to notify the corresponding chip to read out the extremum strip. The pads PRIIN and PRIOUT are used to pass a token in between chips to control when each chip should put data onto the bus and when readout is complete.

In Readout Cycle, the Bus 0-7 lines are changes from input lines to output lines. During readout, data from each SVX4 chip is placed on the common bus beginning with the top chip in the daisy chain and proceeding sequentially through the remaining chips. Information is placed on the bus in 8 bit bytes. First the chip ID and then the pipeline cell is read out. Then the address and data information for that chip is read out beginning with the channel nearest the top of the chip, channel 1, and proceeding downward. Priority for the output is passed from the PRIOUT of the first chip to the PRIIN pad of the next chip after the first chip has been completely readout. The top chip will have PRIIN first since the PRIIN pad is internally pulled weakly low to initiate readout. Information is readout using both the high and low transitions of the differential clock. Thus, the channel readout rate is approximately equal to the BECLK clock frequency.

7 Measuring the Performance of the SVX4

This section explores the subtleties of determining the bandwidth and choosing the best setting. It begins with a discussion of expectations of bandwidths, integration time, and setting the bandwidth. Effects of external capacitive load are examined and use of the calibration voltage and gain measurements to obtain a standard for presenting results follows. After this discussion there are warnings about testing with unloaded channels, a likely event when one is just looking at a chip on a hybrid, as well as robustness of the measurement including a word on common mode and control using differential noise measurements. A final word of warning on comparing the results to simulation concludes this section.

8 Miscellaneous Considerations

9 Appendix A

9.1 Measurements of Timing on Various Test Stands

9.1.1 Systems in use

- **The Stimulus Test Stand.** This system is based on a general pattern generator that is quite expensive and rather delicate to program. It is however an off-the-shelf item. It has not been setup is any triggerable manner.
- **The Stand Alone Test Chain.** This used the full test chain for D∅.
- **The PATT Test Stand.** This test stand was used at LBL and the wafer probing station. It uses a text file to download the initialization stream.

9.2 Measurements of the Basic Sequence

Analysis of the basic sequence of signals going to and coming from the SVX4 involves studying the Digitization and Readout Cycles while Acquisition is occurring. Items of interest to observer are the changes that occur at each of the cycle boundaries, the acceptance of a trigger and its handling, and the return of the pipeline cell after readout. For the systems that do not run continuous sequences, it is

useful to examine the start and end of the sequence chain and to compare the state of the various lines before the start and after the end of a sequence burst.

This suggests the following measurements be made:

- **Basic Clock Rate.** A measurement of the clock speed used to drive the sequence of signals going to/coming from the chip is useful in each of the systems. Systems may be able to only change states at a one-half their basic clock rates. This has consequences for the rate at which the FECLK or BECLK may be run in comparison to basic clock rate.
- **Full Sequence.** A snapshot of the full sequence starting with the beginning of the burst of signals going to the SVX4 and ending with the end of the burst gives an overview of which lines make transitions at which points. Detailed timing relationships cannot be easily observed.
- **Preamp Reset.** The reset of the preamp should occur between bunches. This is handles differently on various systems and may affect the results they produce. Measurements of where these transitions occurs have been made.
- **Start of Sequence**. The disposition of the various signal lines at the start of the sequence is relevant for systems that do not run continuously.
- **Level 1 Accept**. The level 1 accept causes the pipeline cell to be put aside.
- **Digitization**. Resetting of the Wilkinson ramp, the counter, the threshold comparators and the interaction with the PRD1 signals which place the pedestal and then the signal capacitor in place for measurement are critical portions of the SVX4 operation and are hence interesting to measure.
- **End of Digitization**. The signaling of the end of the digitization and the observation of the operation of the top and bottom neighbor logic in action are interesting to document.
- **End of Digitization/Beginning of Readout**. The transition from the end of the digitization to the readout, noting the modification of the BEMODE line over this boundary is of interest to document.
- **Beginning of Readout**. Examination of the data lines and correlation of the data with that which are eventually seen in computer memory of the device used to store that data are interesting to study.
- **End of Readout**. The final data words, together with observation of how the data stream to the computer is terminated, are correlated with the data as they appear on the computer.
- **End of Sequence**. The end of the commands sent to the chip for systems which send only bursts of sequences are useful measurements so that the quiescent state of the lines between bursts can be studied.

9.3 The D0 Sequence

The following pictures show the simulation waveforms that were used to test the schematic level design of the SVX4. Both D0 and CDF agreed to choose waveforms that would test most of the features of the SVX4 and to be complementary to each other. One waveform testing one set of features and the other waveform testing orthogonal features. The parameters used for the D0 sequence were as follows:

- Injection mask : 125 injected on only
- Mask disable is off
- Bandwidth settings: 0000
- Bias controls: 0010
- Trigger latency: 13

- Pipeline readout order: signal cell first, then pedestal cell 47
- Chip id: 0
- DPS setting: on
- Channel 127 readout: not read out
- Channel 63 readout: read out
- Sparsify mode: on
- Read neighbors: on
- Ramp pedestal: 0000
- Ramp direction, comparator polarity: both 0
- Ramp range: 000
- Threshold: 20
- Counter modulo: 255
- Note that 46 cycles before the first operation are used to assure that all pipeline cells have valid data (thus the first L1 is issued at the 59^{th} clock pulse (i.e. 46 +13 for trigger latency)
- **WARNING :** These waveforms were generated and used during the simulation phase of the design of the chip. Similar waveforms have been used for operational testing of the chip but with some significant differences : In the waveforms the CHMODE line is not properly used, for maximum noise immunity this line should be high only during the period that the BEMODE and FEMODE lines are changing. In addition the PRIOUT line during initialization will reflect whatever random state the download register is in after power up (in these simulations that state was set to be the same state as the one we end up in). PRIOUT during initialization will have well defined data only after the chip has been fully loaded, as described earlier in the section where the daisy chaining of chips was discussed.

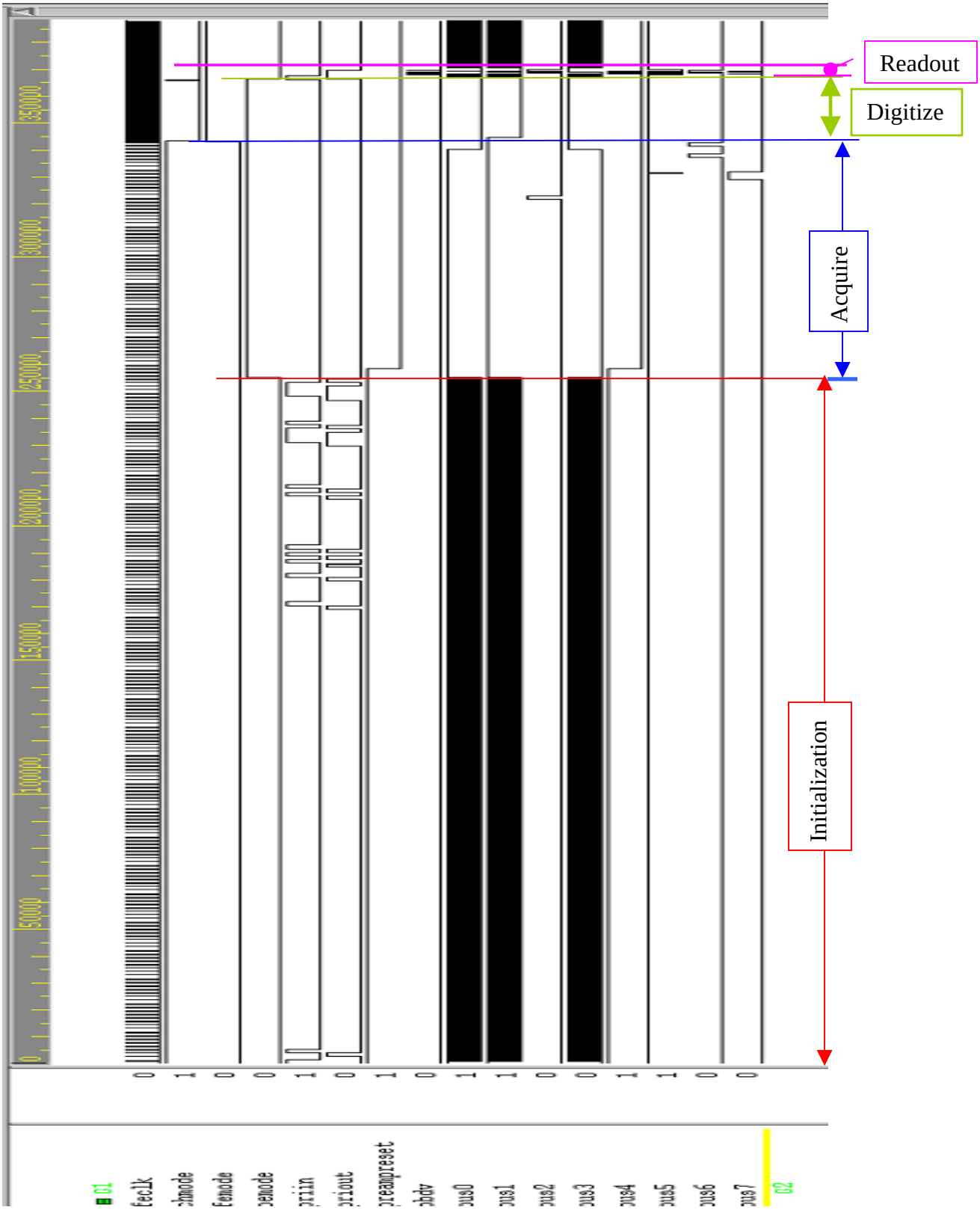

Figure 15 The full D0 waveform using a sparsified setting for readout.

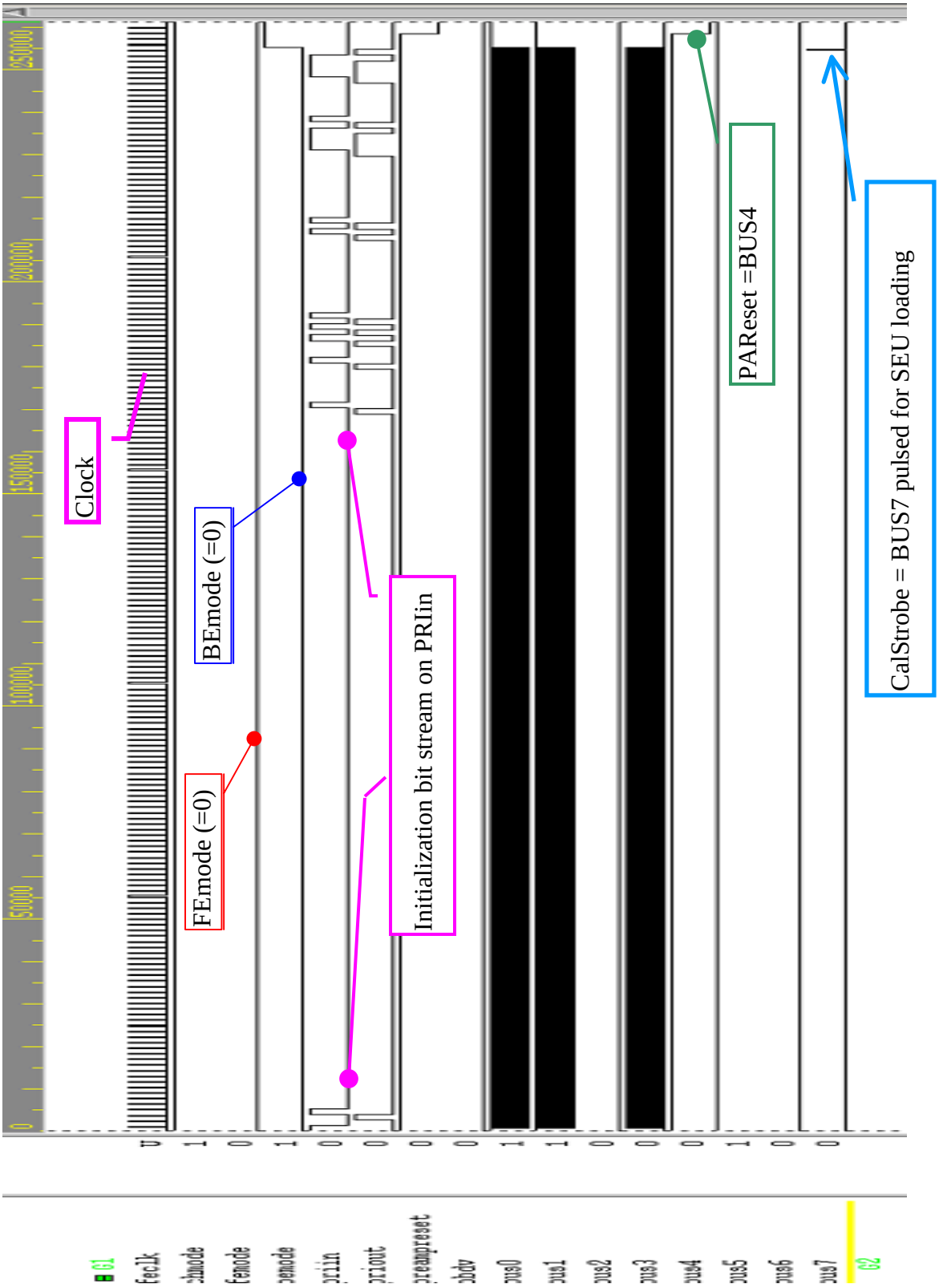

Figure 16 The initialization sequence for D0.

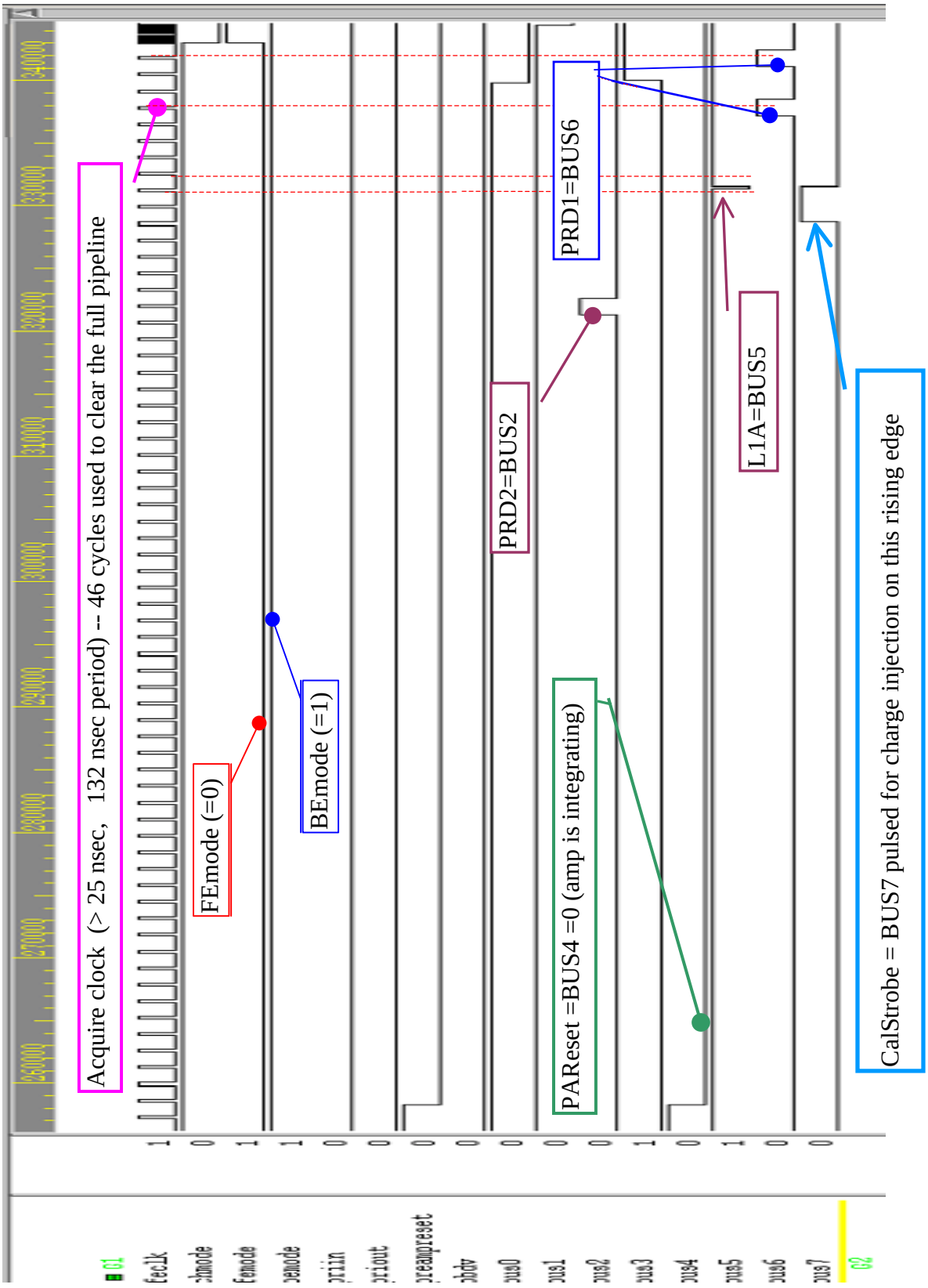

Figure 17 An enlargement of the acquire sequence in the front-end in D0mode.

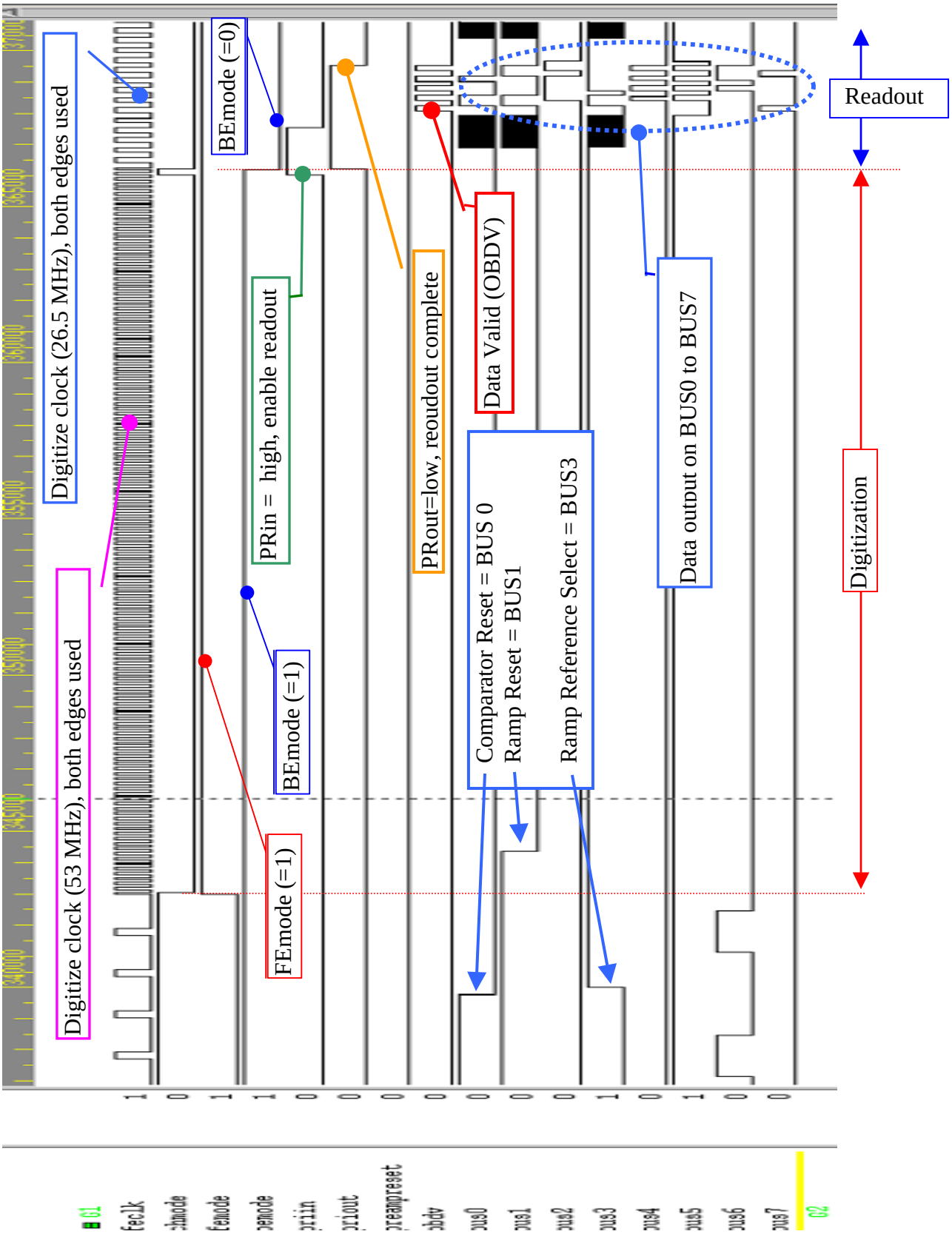

Figure 18 A enlargement of the digitization and readout in sparsify mode for D0.

9.4 The CDF Sequence

The following pictures show the simulation waveforms that were used to test the schematic level design of the SVX4. Both D0 and CDF agreed to choose waveforms that would test most of the features of the SVX4 and to be complementary to each other. One waveform testing one set of features and the other waveform testing orthogonal features. The parameters used for the D0 sequence were as follows:

- Injection mask : every 8^{th} channel
- Mask disable is off
- Bandwidth settings: 1000
- Bias controls: 0010
- Trigger latency: 5
- Pipeline readout order: signal cell first, then pedestal cell 47
- Chip id: 24
- DPS setting: off
- Channel 127 readout: read out
- Channel 63 readout: not read out
- Sparsify mode: on
- Read neighbors: off
- Ramp pedestal: 1000
- Ramp direction, comparator polarity: both 0
- Ramp range: 000
- Threshold: 150
- Counter modulo: 240
- Note that 46 cycles before the first operation are used to assure that all pipeline cells have valid data (thus the first L1 is issued at the 51^{st} clock pulse (i.e. 46 +5 for trigger latency)
- **WARNING :** These waveforms were generated and used during the simulation phase of the design of the chip. Similar waveforms have been used for operational testing of the chip but with some significant differences: In the waveforms the CHMODE line is not properly used, for maximum noise immunity this line should be high only during the period that the BEMODE and FEMODE lines are changing. In addition the PRIOUT line during initialization will reflect whatever random state the download register is in after power up (in these simulations that state was set to be the same state as the one we end up in). PRIOUT during initialization will have well defined data only after the chip has been fully loaded, as described earlier in the section where the daisy chaining of chips was discussed.

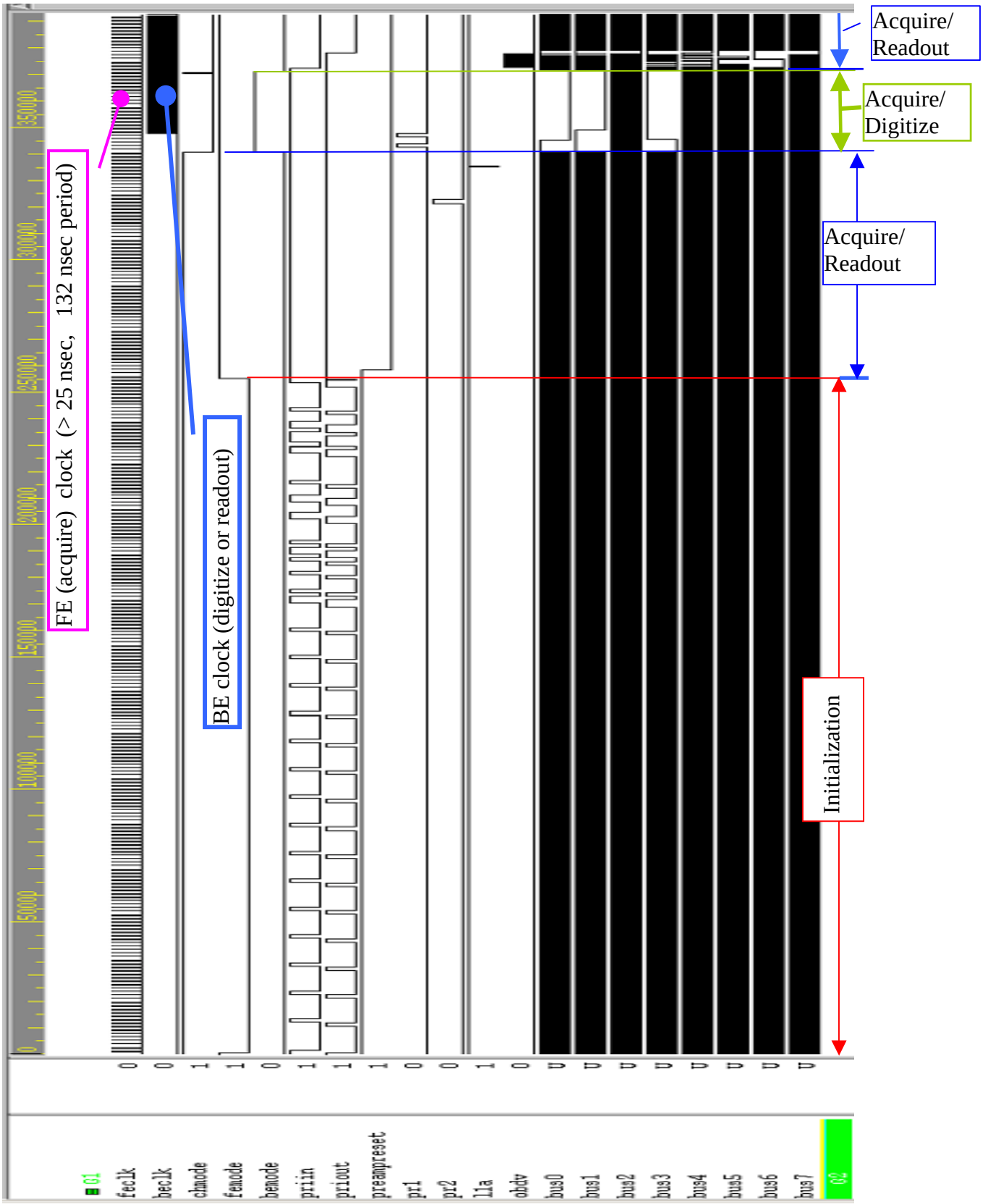

Figure 19 The full CDF sequence in sparsify mode.

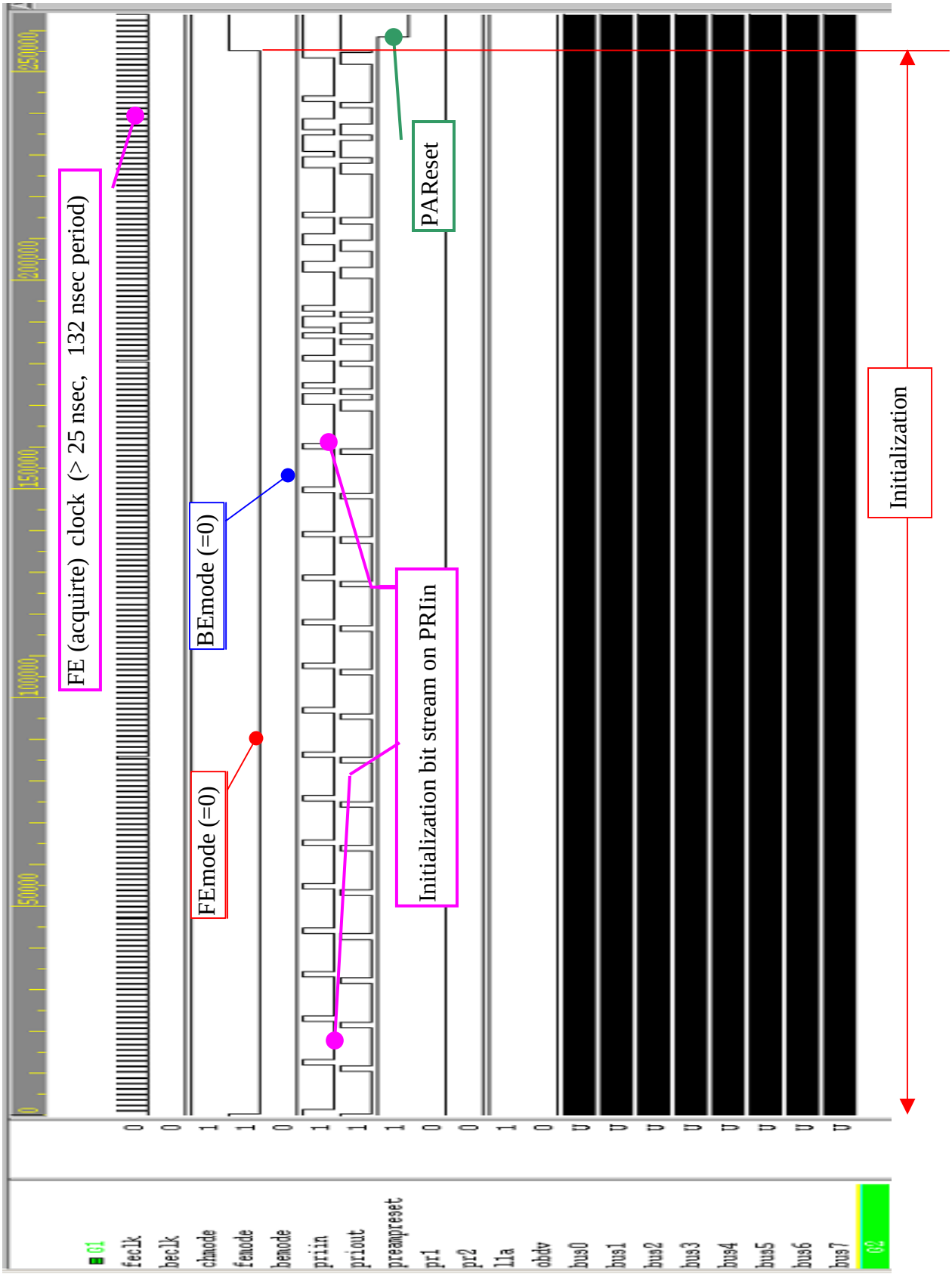

Figure 20 The initialization sequence for CDF mode.

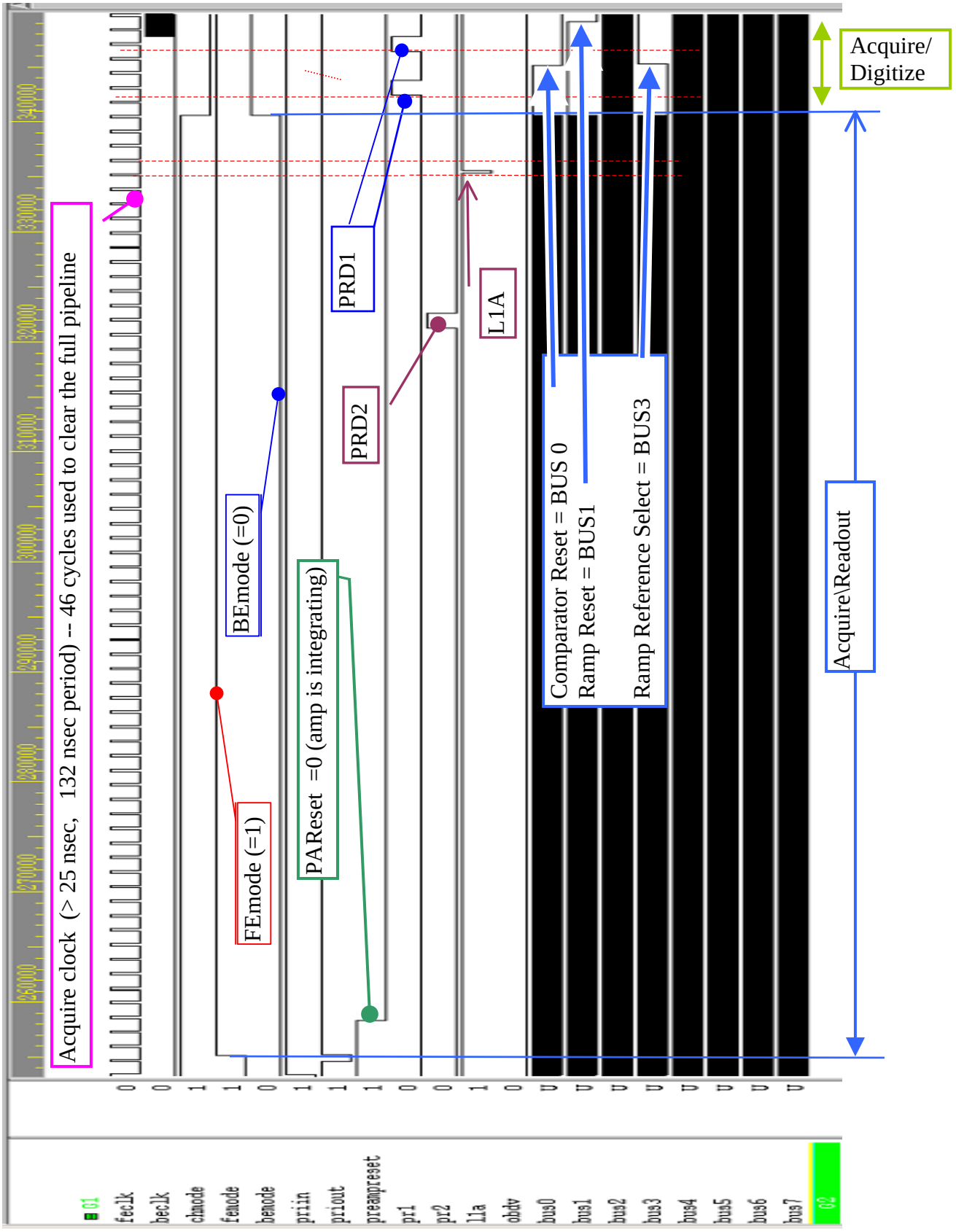

Figure 21 The acquire waveform for CDF.

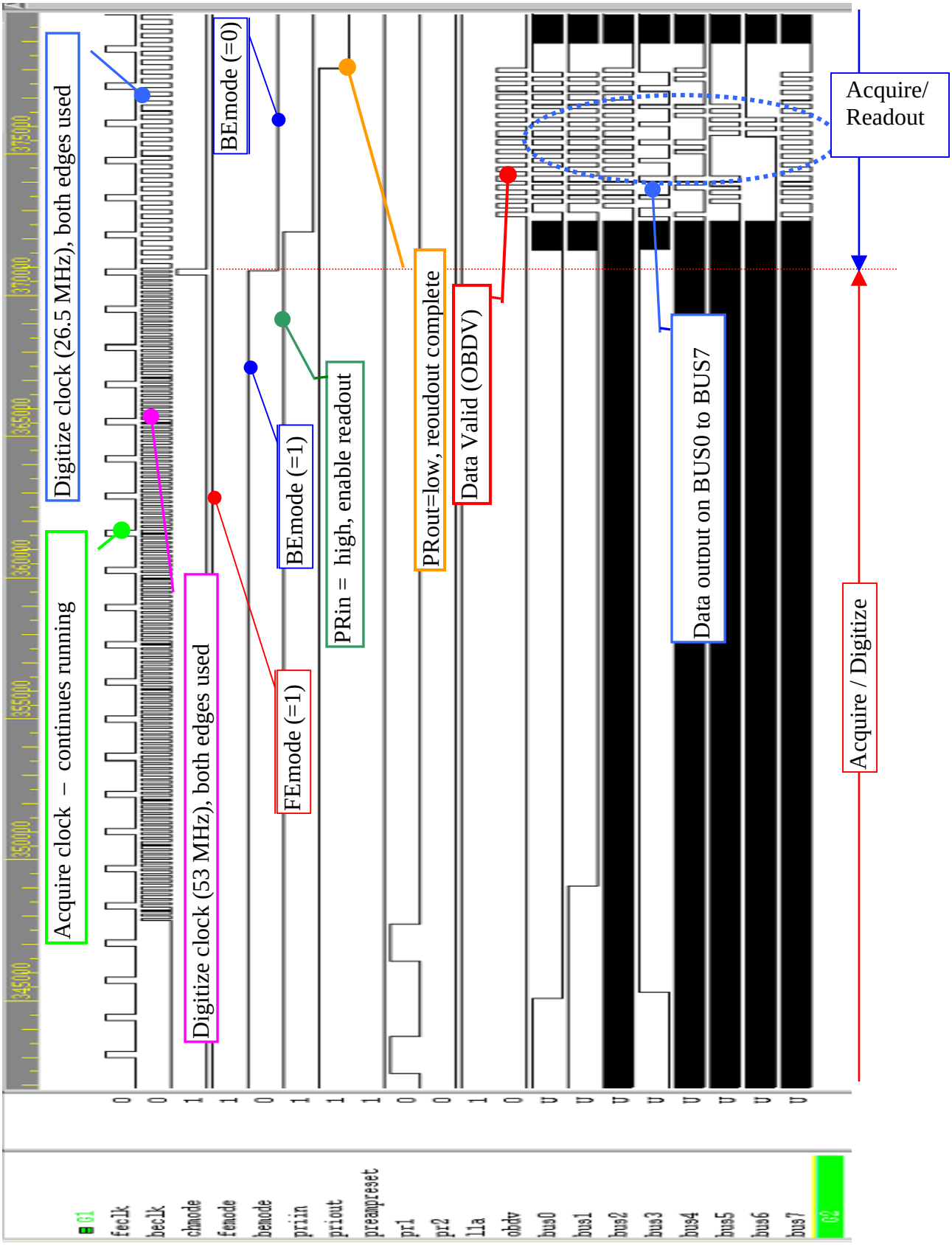

Figure 22 Digitization and readout for CDF mode.

10 Appendix B -The SVX4 Specifications (original list)

This set of specifications was given to the chip designers as the design guideline. To the extent that there are changes between this early set of specs and the text of the rest of the manual – the text of the manual has the correct information.

==========

A. General:

1. Input bonding pad pitch:	48μm
2. Overall Width:	6.250mm active area. Dicing streets as close as allowed by design rules.
3. Overall length:	< 11.925mm
4. Supply voltages:	2.25-2.75V analog, 2.25-2.75V digital.
5. Versions:	A version is the basic "conservative" version. B version adds on-chip bypassing and front to back combined power routing,
6. Bond pad layout:	Both version have same bond pad layout with some pads used only by CDF and others used only by D0.
7. Bond pads:	Except Front End inputs, no wirebond pad is to be smaller than 150x150um (cover layer opening). Probe pads not meant for wirebonding are exempt.
8. Maximum Supply Voltage:	3.5V

B. Preamp:

1. Input pulse polarity:	Positive
2. Gain (feedback capacitor):	3mV/fC
3. Gain uniformity (ch-to-ch):	5% or better
4. External load capacitance:	10pF to 50pF
5. Risetime 0-90%:	adjustable in a range that includes 60-100ns for any allowed load
6. Risetime adjustment:	4 bits minimum
7. Noise (ENC):	2000e or less for a 40pF load using double correlated sampling with 100ns integration t.
8. DC open loop gain:	>2500 (>95% charge collection from 40pF)
9. Linearity:	Linear response for pulses up to 20fC non-linearity < 0.25mV at output
10.Dynamic range:	>200fC
11.Reset + settling time:	<1μs for any initial condition
12.Reset offset voltage:	Internally set to a value TBD by designers, with external override capability.
13.Input protection diodes:	2uA DC capability to either rail. Current must not go to substrate.
14.Calibration injection:	40fF internal cap switched to input
15.Calibration charge control:	1 external analog reference voltage (other voltage is AVDD, not ground)
17. Input disable switch:	2 Config. Register bits. #1 disables control of reset switch for channel with calibration mask bit set. #2 determines whether reset switch is always closed or always open for disabled

	channels.
18.Input Device Current:	Adjustable with configuration bits as in SVX3 but with wider range (factor of 2).
19.Bypass capacitors:	Performance in SVX-II mode should be maintained with no external bypass capacitors closer than 10mm.

C. Pipeline:

1. Input Pulse polarity:	Negative
2. Voltage gain:	3 to 5
3. Gain uniformity:	5% channel to channel
4. Risetime, 0-90%:	10ns to 40ns (in that range, fixed)
5. Noise (ENC at preamp input)	<500e
6. Linearity:	linear response up to 20fC at preamp input
7. Dynamic Range:	To Be Confirmed: >40fC at preamp input
8. Reset Time:	<20ns for any allowed initial condition
9. Pedestal uniformity:	<500e at preamp input channel to channel <1000e at preamp input cell to cell
10. Bias:	Internally set with override bonding pad.

D. ADC:

1. Type:	Wilkinson with real time pedestal subtraction.
2. Voltage Ramp:	Rate adjustable with external resistor.
3. Ramp rate "trim" bits:	3 Bits, adding binary weighted capacitors to op-amp feedback. Largest capacitor is 4x the fixed feedback capacitor. These capacitors provide a range adjustment- no fine adjustment needed.
4. Ramp Linearity:	0.25% for rates between 0.1 and 1 V/us.
5. Ramp dynamic range:	1V
6. Ramp pedestal:	Same as in SVX3.
7. Counter:	8-bit Gray code, 106MHz rate.
8. Differential nonlinearity:	<0.5 LSB.
9. Bias:	Internally set with override bonding pad

E. Data output drivers:

1. Type:	Complementary with "resistor current sources"
2. Current source range:	2.5mA to 17.5mA in 2.5mA steps (3 bit adjust).
3. Rise and fall times:	>2ns and <4ns with nominal load.
4. Common mode:	VDD/2 nominal with T termination.
5: Load capability:	70ohm and 20pF.
7. Tri-state:	Outputs tristated in initialize (except if SR copy pad is bonded- see H7) and digitize modes.
8. Single ended use:	No additional requirements
9. Bi-directional:	All Bus pads will be bi-directional. Only some will be used of input as well as output by CDF, but all of them will be I/O for D0.
10. Output data skew:	<3ns between OBDV and any bus line and between any two bus lines.

F. TN/BN Pins:

1. Functions	The multiplexed functions of the SVX3 TN/BN pads will be separated in SVX4 to TN/BN and Priority in/out dedicated sets of pads.
2. Type, BN/TN:	"Open collector" I/O with internal pull-up.
3. Type, Priority in:	Differential receiver (2 bond pads) same as clock receivers, with added high Z common mode reference voltage (center tap of large resistance between power and ground).
4. Type, Priority out:	Differential driver (2 bond pads) same as data bus outputs.
5. BN/TN Internal pull-up:	>500 ohm
6. BN/TN Pull-down current:	>10mA
7. BN/TN Modes:	only active in digitize mode
8. Priority in/out Modes:	Configuration register input/output during initialize mode. Priority passing during readout mode. Priority out high during digitize mode.
9. Bonding pads:	This increases the number of bonding pads per chip by 4 (2 next to TN and 2 next to BN).

G. Configuration Register:

1. Type:	Bit serial shift register.
2. Cell type:	SEU tolerant shadow register.
3. Shadow register:	Keep for SEU tolerance.
4. Clock:	Register advanced with FE clock in initialize mode.
5. Length:	no limit.
6. Preset:	no preset.
7. layout rule:	Do not place configuration register cells within 75um of a wirebond pad (they tend to be destroyed by missed wirebonds).
8. Bit order:	LSB loads first on all fields.
9. Bit Assignment:	Numbers are for illustration. Designers may add bias adjust or other system bits as needed.

0-127:	Calibration Mask
128:	Cal-inject signal polarity
129:	Input disable
130:	Disable mode (reset always on or off)
140-144:	Bandwidth bits (left room for 5)
145-147:	Input transistor current
148-153:	Pipeline depth
154:	Pipeline readout order
155-161:	Chip ID
162:	Real time pedestal subtraction Enable
163:	Last channel latch
164:	Channel 63 latch
165:	Read all
166:	Read Neighbors
167-170:	Ramp pedestal
171:	Ramp direction
172:	Comparator polarity

173-175: Ramp range selection
176-183: Sparsification threshold
184-191: Counter Modulo
192: First chip flag (see H.9)
193: Last chip flag (see H.9)
192-194: Output driver resistor select

H. Control Functions:

(*) Denotes desirable feature but not strictly required

1. Signal Functions: All control signals same function as SVX3 except as noted here.

2. Ramp and Counter Reset: Remove Counter Reset as an independent signal. In normal mode Counter Reset is to be tied to Ramp Reset. In Dynamic Pedestal Subtraction mode Counter Reset is internally generated as in SVX3.

3. Preamp Reset & Fe Clock: Preamp Reset should always function independently of FE Clock state. In SVX3 Preamp Reset can only go high while FE Clock is high.

4. PRD2 (*): It is desirable that PRD2 control only the acquisition of the reference capacitor pedestal, and that the action of returning a cell to the pipeline be automatically triggered by the end of digitization (The falling edge of DIGITIZE MODE is used to drive the MOVE DATA pipeline input)

5. Last channel SR bit: on=always latch chan. 127 (same "last chip flag" in SVX3).

6. Chan. 63 latch SR bit (*): on=always latch chan. 63 (doubles read out speed)

7. Bus 3 SR copy bond pad: copy Priority out in initialize mode to Bus 3 output if pad is bonded to ground (and enable output bus in init. mode)

8. extra L1A: Additional L1A pulses (beyond 4) should be ignored by the pipeline logic.

9. OBDV(data valid)control(*): OBDV must be driven by 1 chip per daisy chain at all times to prevent data transmission errors. This can be accomplished in SVX4 with 2 configuration register bits: First Chip (FC) and Last Chip (Different from item 5). OBDV control is given by the following logic table

Pri. In	Pri. Out	FC	LC	OBDV
H	H	L	L	disabled
H	L	L	L	disabled
L	H	L	L	ENABLED
L	L	L	L	disabled*
X	H	H	L	ENABLED
X	L	H	L	disabled*
H	X	L	H	disabled
L	X	L	H	ENABLED

*OBDV is to be disabled one BE_CLOCK cycle after Pri. Out is lowered (same as in SVX3). [In the present CDF silicon system it was necessary to add logic to the port cards to implement this function, because the SVX3 does not have the FC and LC bits.]

10. Readout Mode Pad: Add an output pad to make the "Readout Mode" internal signal available

11. D0 Mode pad:	A special bond pad, if left un-bonded will set the chip in D0 mode. This will multiplex I/O signals onto all Bus lines and gate the Pipeline Clock off during digitize and readout operations.
12. Test outputs:	Buffered preamp and pipeline outputs for one channel, Comparator output for 1 channel, Ramp probe point, RTPS comparator buffered input And output- all as in SVX3. Additional probe points as needed to fully test performance.

11 Appendix C - Decimal/Gray tables

Decimal to Gray code					
Dec	Hex	Binary	Bits	"Hex"	"Dec"
0	0	0	0	0	0
1	1	1	1	1	1
2	2	10	11	3	3
3	3	11	10	2	2
4	4	100	110	6	6
5	5	101	111	7	7
6	6	110	101	5	5
7	7	111	100	4	4
8	8	1000	1100	C	12
9	9	1001	1101	D	13
10	A	1010	1111	F	15
11	B	1011	1110	E	14
12	C	1100	1010	A	10
13	D	1101	1011	B	11
14	E	1110	1001	9	9
15	F	1111	1000	8	8
16	10	10000	11000	18	24
17	11	10001	11001	19	25
18	12	10010	11011	1B	27
19	13	10011	11010	1A	26
20	14	10100	11110	1E	30
21	15	10101	11111	1F	31
22	16	10110	11101	1D	29
23	17	10111	11100	1C	28
24	18	11000	10100	14	20
25	19	11001	10101	15	21
26	1A	11010	10111	17	23
27	1B	11011	10110	16	22
28	1C	11100	10010	12	18
29	1D	11101	10011	13	19
30	1E	11110	10001	11	17
31	1F	11111	10000	10	16
32	20	100000	110000	30	48
33	21	100001	110001	31	49
34	22	100010	110011	33	51
35	23	100011	110010	32	50
36	24	100100	110110	36	54
37	25	100101	110111	37	55
38	26	100110	110101	35	53
39	27	100111	110100	34	52
40	28	101000	111100	3C	60

Gray Code to Decimal					
"Hex"	"Dec"	Bits	Binary	Hex	Dec
0	0	0	0	0	0
1	1	1	1	1	1
2	2	10	11	3	3
3	3	11	10	2	2
4	4	100	111	7	7
5	5	101	110	6	6
6	6	110	100	4	4
7	7	111	101	5	5
8	8	1000	1111	F	15
9	9	1001	1110	E	14
10	A	1010	1100	C	12
11	B	1011	1101	D	13
12	C	1100	1000	8	8
13	D	1101	1001	9	9
14	E	1110	1011	B	11
15	F	1111	1010	A	10
16	10	10000	11111	1F	31
17	11	10001	11110	1E	30
18	12	10010	11100	1C	28
19	13	10011	11101	1D	29
20	14	10100	11000	18	24
21	15	10101	11001	19	25
22	16	10110	11011	1B	27
23	17	10111	11010	1A	26
24	18	11000	10000	10	16
25	19	11001	10001	11	17
26	1A	11010	10011	13	19
27	1B	11011	10010	12	18
28	1C	11100	10111	17	23
29	1D	11101	10110	16	22
30	1E	11110	10100	14	20
31	1F	11111	10101	15	21
32	20	100000	111111	3F	63
33	21	100001	111110	3E	62
34	22	100010	111100	3C	60
35	23	100011	111101	3D	61
36	24	100100	111000	38	56
37	25	100101	111001	39	57
38	26	100110	111011	3B	59
39	27	100111	111010	3A	58
40	28	101000	110000	30	48

Decimal to Gray code					
Dec	Hex	Binary	Bits	"Hex"	"Dec"
41	29	101001	111101	3D	61
42	2A	101010	111111	3F	63
43	2B	101011	111110	3E	62
44	2C	101100	111010	3A	58
45	2D	101101	111011	3B	59
46	2E	101110	111001	39	57
47	2F	101111	111000	38	56
48	30	110000	101000	28	40
49	31	110001	101001	29	41
50	32	110010	101011	2B	43
51	33	110011	101010	2A	42
52	34	110100	101110	2E	46
53	35	110101	101111	2F	47
54	36	110110	101101	2D	45
55	37	110111	101100	2C	44
56	38	111000	100100	24	36
57	39	111001	100101	25	37
58	3A	111010	100111	27	39
59	3B	111011	100110	26	38
60	3C	111100	100010	22	34
61	3D	111101	100011	23	35
62	3E	111110	100001	21	33
63	3F	111111	100000	20	32
64	40	1000000	1100000	60	96
65	41	1000001	1100001	61	97
66	42	1000010	1100011	63	99
67	43	1000011	1100010	62	98
68	44	1000100	1100110	66	102
69	45	1000101	1100111	67	103
70	46	1000110	1100101	65	101
71	47	1000111	1100100	64	100
72	48	1001000	1101100	6C	108
73	49	1001001	1101101	6D	109
74	4A	1001010	1101111	6F	111
75	4B	1001011	1101110	6E	110
76	4C	1001100	1101010	6A	106
77	4D	1001101	1101011	6B	107
78	4E	1001110	1101001	69	105
79	4F	1001111	1101000	68	104
80	50	1010000	1111000	78	120
81	51	1010001	1111001	79	121
82	52	1010010	1111011	7B	123
83	53	1010011	1111010	7A	122
84	54	1010100	1111110	7E	126

Gray Code to Decimal					
"Hex"	"Dec"	Bits	Binary	Hex	Dec
41	29	101001	110001	31	49
42	2A	101010	110011	33	51
43	2B	101011	110010	32	50
44	2C	101100	110111	37	55
45	2D	101101	110110	36	54
46	2E	101110	110100	34	52
47	2F	101111	110101	35	53
48	30	110000	100000	20	32
49	31	110001	100001	21	33
50	32	110010	100011	23	35
51	33	110011	100010	22	34
52	34	110100	100111	27	39
53	35	110101	100110	26	38
54	36	110110	100100	24	36
55	37	110111	100101	25	37
56	38	111000	101111	2F	47
57	39	111001	101110	2E	46
58	3A	111010	101100	2C	44
59	3B	111011	101101	2D	45
60	3C	111100	101000	28	40
61	3D	111101	101001	29	41
62	3E	111110	101011	2B	43
63	3F	111111	101010	2A	42
64	40	1000000	1111111	7F	127
65	41	1000001	1111110	7E	126
66	42	1000010	1111100	7C	124
67	43	1000011	1111101	7D	125
68	44	1000100	1111000	78	120
69	45	1000101	1111001	79	121
70	46	1000110	1111011	7B	123
71	47	1000111	1111010	7A	122
72	48	1001000	1110000	70	112
73	49	1001001	1110001	71	113
74	4A	1001010	1110011	73	115
75	4B	1001011	1110010	72	114
76	4C	1001100	1110111	77	119
77	4D	1001101	1110110	76	118
78	4E	1001110	1110100	74	116
79	4F	1001111	1110101	75	117
80	50	1010000	1100000	60	96
81	51	1010001	1100001	61	97
82	52	1010010	1100011	63	99
83	53	1010011	1100010	62	98
84	54	1010100	1100111	67	103

Decimal to Gray code					
Dec	Hex	Binary	Bits	"Hex"	"Dec"
85	55	1010101	1111111	7F	127
86	56	1010110	1111101	7D	125
87	57	1010111	1111100	7C	124
88	58	1011000	1110100	74	116
89	59	1011001	1110101	75	117
90	5A	1011010	1110111	77	119
91	5B	1011011	1110110	76	118
92	5C	1011100	1110010	72	114
93	5D	1011101	1110011	73	115
94	5E	1011110	1110001	71	113
95	5F	1011111	1110000	70	112
96	60	1100000	1010000	50	80
97	61	1100001	1010001	51	81
98	62	1100010	1010011	53	83
99	63	1100011	1010010	52	82
100	64	1100100	1010110	56	86
101	65	1100101	1010111	57	87
102	66	1100110	1010101	55	85
103	67	1100111	1010100	54	84
104	68	1101000	1011100	5C	92
105	69	1101001	1011101	5D	93
106	6A	1101010	1011111	5F	95
107	6B	1101011	1011110	5E	94
108	6C	1101100	1011010	5A	90
109	6D	1101101	1011011	5B	91
110	6E	1101110	1011001	59	89
111	6F	1101111	1011000	58	88
112	70	1110000	1001000	48	72
113	71	1110001	1001001	49	73
114	72	1110010	1001011	4B	75
115	73	1110011	1001010	4A	74
116	74	1110100	1001110	4E	78
117	75	1110101	1001111	4F	79
118	76	1110110	1001101	4D	77
119	77	1110111	1001100	4C	76
120	78	1111000	1000100	44	68
121	79	1111001	1000101	45	69
122	7A	1111010	1000111	47	71
123	7B	1111011	1000110	46	70
124	7C	1111100	1000010	42	66
125	7D	1111101	1000011	43	67
126	7E	1111110	1000001	41	65
127	7F	1111111	1000000	40	64
128	80	10000000	11000000	C0	192

Gray Code to Decimal					
"Hex"	"Dec"	Bits	Binary	Hex	Dec
85	55	1010101	1100110	66	102
86	56	1010110	1100100	64	100
87	57	1010111	1100101	65	101
88	58	1011000	1101111	6F	111
89	59	1011001	1101110	6E	110
90	5A	1011010	1101100	6C	108
91	5B	1011011	1101101	6D	109
92	5C	1011100	1101000	68	104
93	5D	1011101	1101001	69	105
94	5E	1011110	1101011	6B	107
95	5F	1011111	1101010	6A	106
96	60	1100000	1000000	40	64
97	61	1100001	1000001	41	65
98	62	1100010	1000011	43	67
99	63	1100011	1000010	42	66
100	64	1100100	1000111	47	71
101	65	1100101	1000110	46	70
102	66	1100110	1000100	44	68
103	67	1100111	1000101	45	69
104	68	1101000	1001111	4F	79
105	69	1101001	1001110	4E	78
106	6A	1101010	1001100	4C	76
107	6B	1101011	1001101	4D	77
108	6C	1101100	1001000	48	72
109	6D	1101101	1001001	49	73
110	6E	1101110	1001011	4B	75
111	6F	1101111	1001010	4A	74
112	70	1110000	1011111	5F	95
113	71	1110001	1011110	5E	94
114	72	1110010	1011100	5C	92
115	73	1110011	1011101	5D	93
116	74	1110100	1011000	58	88
117	75	1110101	1011001	59	89
118	76	1110110	1011011	5B	91
119	77	1110111	1011010	5A	90
120	78	1111000	1010000	50	80
121	79	1111001	1010001	51	81
122	7A	1111010	1010011	53	83
123	7B	1111011	1010010	52	82
124	7C	1111100	1010111	57	87
125	7D	1111101	1010110	56	86
126	7E	1111110	1010100	54	84
127	7F	1111111	1010101	55	85
128	80	10000000	11111111	FF	255

Decimal to Gray code					
Dec	Hex	Binary	Bits	"Hex"	"Dec"
129	81	10000001	11000001	C1	193
130	82	10000010	11000011	C3	195
131	83	10000011	11000010	C2	194
132	84	10000100	11000110	C6	198
133	85	10000101	11000111	C7	199
134	86	10000110	11000101	C5	197
135	87	10000111	11000100	C4	196
136	88	10001000	11001100	CC	204
137	89	10001001	11001101	CD	205
138	8A	10001010	11001111	CF	207
139	8B	10001011	11001110	CE	206
140	8C	10001100	11001010	CA	202
141	8D	10001101	11001011	CB	203
142	8E	10001110	11001001	C9	201
143	8F	10001111	11001000	C8	200
144	90	10010000	11011000	D8	216
145	91	10010001	11011001	D9	217
146	92	10010010	11011011	DB	219
147	93	10010011	11011010	DA	218
148	94	10010100	11011110	DE	222
149	95	10010101	11011111	DF	223
150	96	10010110	11011101	DD	221
151	97	10010111	11011100	DC	220
152	98	10011000	11010100	D4	212
153	99	10011001	11010101	D5	213
154	9A	10011010	11010111	D7	215
155	9B	10011011	11010110	D6	214
156	9C	10011100	11010010	D2	210
157	9D	10011101	11010011	D3	211
158	9E	10011110	11010001	D1	209
159	9F	10011111	11010000	D0	208
160	A0	10100000	11110000	F0	240
161	A1	10100001	11110001	F1	241
162	A2	10100010	11110011	F3	243
163	A3	10100011	11110010	F2	242
164	A4	10100100	11110110	F6	246
165	A5	10100101	11110111	F7	247
166	A6	10100110	11110101	F5	245
167	A7	10100111	11110100	F4	244
168	A8	10101000	11111100	FC	252
169	A9	10101001	11111101	FD	253
170	AA	10101010	11111111	FF	255
171	AB	10101011	11111110	FE	254
172	AC	10101100	11111010	FA	250

Gray Code to Decimal					
"Hex"	"Dec"	Bits	Binary	Hex	Dec
129	81	10000001	11111110	FE	254
130	82	10000010	11111100	FC	252
131	83	10000011	11111101	FD	253
132	84	10000100	11111000	F8	248
133	85	10000101	11111001	F9	249
134	86	10000110	11111011	FB	251
135	87	10000111	11111010	FA	250
136	88	10001000	11110000	F0	240
137	89	10001001	11110001	F1	241
138	8A	10001010	11110011	F3	243
139	8B	10001011	11110010	F2	242
140	8C	10001100	11110111	F7	247
141	8D	10001101	11110110	F6	246
142	8E	10001110	11110100	F4	244
143	8F	10001111	11110101	F5	245
144	90	10010000	11100000	E0	224
145	91	10010001	11100001	E1	225
146	92	10010010	11100011	E3	227
147	93	10010011	11100010	E2	226
148	94	10010100	11100111	E7	231
149	95	10010101	11100110	E6	230
150	96	10010110	11100100	E4	228
151	97	10010111	11100101	E5	229
152	98	10011000	11101111	EF	239
153	99	10011001	11101110	EE	238
154	9A	10011010	11101100	EC	236
155	9B	10011011	11101101	ED	237
156	9C	10011100	11101000	E8	232
157	9D	10011101	11101001	E9	233
158	9E	10011110	11101011	EB	235
159	9F	10011111	11101010	EA	234
160	A0	10100000	11000000	C0	192
161	A1	10100001	11000001	C1	193
162	A2	10100010	11000011	C3	195
163	A3	10100011	11000010	C2	194
164	A4	10100100	11000111	C7	199
165	A5	10100101	11000110	C6	198
166	A6	10100110	11000100	C4	196
167	A7	10100111	11000101	C5	197
168	A8	10101000	11001111	CF	207
169	A9	10101001	11001110	CE	206
170	AA	10101010	11001100	CC	204
171	AB	10101011	11001101	CD	205
172	AC	10101100	11001000	C8	200

Decimal to Gray code					
Dec	Hex	Binary	Bits	"Hex"	"Dec"
173	AD	10101101	11111011	FB	251
174	AE	10101110	11111001	F9	249
175	AF	10101111	11111000	F8	248
179	B3	10110011	11101010	EA	234
180	B4	10110100	11101110	EE	238
181	B5	10110101	11101111	EF	239
182	B6	10110110	11101101	ED	237
183	B7	10110111	11101100	EC	236
184	B8	10111000	11100100	E4	228
185	B9	10111001	11100101	E5	229
186	BA	10111010	11100111	E7	231
187	BB	10111011	11100110	E6	230
188	BC	10111100	11100010	E2	226
189	BD	10111101	11100011	E3	227
190	BE	10111110	11100001	E1	225
191	BF	10111111	11100000	E0	224
192	C0	11000000	10100000	A0	160
193	C1	11000001	10100001	A1	161
194	C2	11000010	10100011	A3	163
195	C3	11000011	10100010	A2	162
196	C4	11000100	10100110	A6	166
197	C5	11000101	10100111	A7	167
198	C6	11000110	10100101	A5	165
199	C7	11000111	10100100	A4	164
200	C8	11001000	10101100	AC	172
201	C9	11001001	10101101	AD	173
202	CA	11001010	10101111	AF	175
203	CB	11001011	10101110	AE	174
204	CC	11001100	10101010	AA	170
205	CD	11001101	10101011	AB	171
206	CE	11001110	10101001	A9	169
207	CF	11001111	10101000	A8	168
208	D0	11010000	10111000	B8	184
209	D1	11010001	10111001	B9	185
210	D2	11010010	10111011	BB	187
211	D3	11010011	10111010	BA	186
212	D4	11010100	10111110	BE	190
213	D5	11010101	10111111	BF	191
214	D6	11010110	10111101	BD	189
215	D7	11010111	10111100	BC	188
216	D8	11011000	10110100	B4	180
217	D9	11011001	10110101	B5	181
218	DA	11011010	10110111	B7	183
219	DB	11011011	10110110	B6	182

Gray Code to Decimal					
"Hex"	"Dec"	Bits	Binary	Hex	Dec
173	AD	10101101	11001001	C9	201
174	AE	10101110	11001011	CB	203
175	AF	10101111	11001010	CA	202
179	B3	10110011	11011101	DD	221
180	B4	10110100	11011000	D8	216
181	B5	10110101	11011001	D9	217
182	B6	10110110	11011011	DB	219
183	B7	10110111	11011010	DA	218
184	B8	10111000	11010000	D0	208
185	B9	10111001	11010001	D1	209
186	BA	10111010	11010011	D3	211
187	BB	10111011	11010010	D2	210
188	BC	10111100	11010111	D7	215
189	BD	10111101	11010110	D6	214
190	BE	10111110	11010100	D4	212
191	BF	10111111	11010101	D5	213
192	C0	11000000	10000000	80	128
193	C1	11000001	10000001	81	129
194	C2	11000010	10000011	83	131
195	C3	11000011	10000010	82	130
196	C4	11000100	10000111	87	135
197	C5	11000101	10000110	86	134
198	C6	11000110	10000100	84	132
199	C7	11000111	10000101	85	133
200	C8	11001000	10001111	8F	143
201	C9	11001001	10001110	8E	142
202	CA	11001010	10001100	8C	140
203	CB	11001011	10001101	8D	141
204	CC	11001100	10001000	88	136
205	CD	11001101	10001001	89	137
206	CE	11001110	10001011	8B	139
207	CF	11001111	10001010	8A	138
208	D0	11010000	10011111	9F	159
209	D1	11010001	10011110	9E	158
210	D2	11010010	10011100	9C	156
211	D3	11010011	10011101	9D	157
212	D4	11010100	10011000	98	152
213	D5	11010101	10011001	99	153
214	D6	11010110	10011011	9B	155
215	D7	11010111	10011010	9A	154
216	D8	11011000	10010000	90	144
217	D9	11011001	10010001	91	145
218	DA	11011010	10010011	93	147
219	DB	11011011	10010010	92	146

Decimal to Gray code					
Dec	Hex	Binary	Bits	"Hex"	"Dec"
220	DC	11011100	10110010	B2	178
221	DD	11011101	10110011	B3	179
222	DE	11011110	10110001	B1	177
223	DF	11011111	10110000	B0	176
224	E0	11100000	10010000	90	144
225	E1	11100001	10010001	91	145
226	E2	11100010	10010011	93	147
227	E3	11100011	10010010	92	146
228	E4	11100100	10010110	96	150
229	E5	11100101	10010111	97	151
230	E6	11100110	10010101	95	149
231	E7	11100111	10010100	94	148
232	E8	11101000	10011100	9C	156
233	E9	11101001	10011101	9D	157
234	EA	11101010	10011111	9F	159
235	EB	11101011	10011110	9E	158
236	EC	11101100	10011010	9A	154
237	ED	11101101	10011011	9B	155
238	EE	11101110	10011001	99	153
239	EF	11101111	10011000	98	152
240	F0	11110000	10001000	88	136
241	F1	11110001	10001001	89	137
242	F2	11110010	10001011	8B	139
243	F3	11110011	10001010	8A	138
244	F4	11110100	10001110	8E	142
245	F5	11110101	10001111	8F	143
246	F6	11110110	10001101	8D	141
247	F7	11110111	10001100	8C	140
248	F8	11111000	10000100	84	132
249	F9	11111001	10000101	85	133
250	FA	11111010	10000111	87	135
251	FB	11111011	10000110	86	134
252	FC	11111100	10000010	82	130
253	FD	11111101	10000011	83	131
254	FE	11111110	10000001	81	129
255	FF	11111111	10000000	80	128

Gray Code to Decimal					
"Hex"	"Dec"	Bits	Binary	Hex	Dec
220	DC	11011100	10010111	97	151
221	DD	11011101	10010110	96	150
222	DE	11011110	10010100	94	148
223	DF	11011111	10010101	95	149
224	E0	11100000	10111111	BF	191
225	E1	11100001	10111110	BE	190
226	E2	11100010	10111100	BC	188
227	E3	11100011	10111101	BD	189
228	E4	11100100	10111000	B8	184
229	E5	11100101	10111001	B9	185
230	E6	11100110	10111011	BB	187
231	E7	11100111	10111010	BA	186
232	E8	11101000	10110000	B0	176
233	E9	11101001	10110001	B1	177
234	EA	11101010	10110011	B3	179
235	EB	11101011	10110010	B2	178
236	EC	11101100	10110111	B7	183
237	ED	11101101	10110110	B6	182
238	EE	11101110	10110100	B4	180
239	EF	11101111	10110101	B5	181
240	F0	11110000	10100000	A0	160
241	F1	11110001	10100001	A1	161
242	F2	11110010	10100011	A3	163
243	F3	11110011	10100010	A2	162
244	F4	11110100	10100111	A7	167
245	F5	11110101	10100110	A6	166
246	F6	11110110	10100100	A4	164
247	F7	11110111	10100101	A5	165
248	F8	11111000	10101111	AF	175
249	F9	11111001	10101110	AE	174
250	FA	11111010	10101100	AC	172
251	FB	11111011	10101101	AD	173
252	FC	11111100	10101000	A8	168
253	FD	11111101	10101001	A9	169
254	FE	11111110	10101011	AB	171
255	FF	11111111	10101010	AA	170

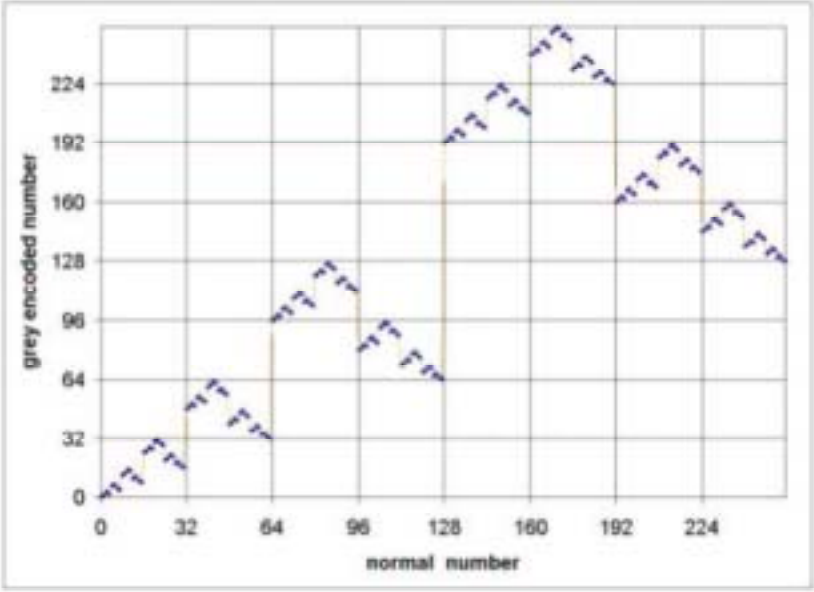

Figure 23 Gray vs normal number. A pattern familiar to persons debugging the SVX chips, it appear for channel Id's of the SVX4 in read-all mode if one byte is missing during readout.

12 References

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